Sparrow: A new broadband software radio development platform

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Overview

• Digitization architectures for astronomy
• Common problems with the existing approach
• Advantages of digitising at the antenna
• The Sparrow project
• Current Status
• Future Fun
Low-Frequency Digitization Architectures

• Cheap, numerous, antennas
• Low bandwidth $O(100 \text{ MHz})$
• Little station-level (per-antenna) processing

→ Easy to process many antennas in a single FPGA
Example: Architecture for HERA

Node (1 of 30)
- FE power
- PA power
- SNAP board
- ADCs
- F

Container
- WR switch
- 1 PPS
- 10 MHz
- SPA
- Control server

Transformer
- 3.3kV - 400V
- 50 kVA

4 x 40 GbE Switch

Public data products

Karoo Array Processing Building
- Control server
- Data Recorder
- Real-Time Processor
- Librarian
- Quality Assurance
- Off-line Processing

Data & Analysis NRAO

Internet

Public data products
Why this “Many antennas per board” architecture?

• Reduces size of clock distribution problem
• [supposed to be] cost-effective

<table>
<thead>
<tr>
<th>Platform</th>
<th>Capability (# inputs × sampling rate)</th>
<th>Used by</th>
<th>Cost/Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROACH2 + 2 x ADC16</td>
<td>$32 \times 250 \text{ Msp} \text{s or } 16 \times 500 \text{ Msp} \text{s} $</td>
<td>LEDA, PAPER</td>
<td>$400</td>
</tr>
<tr>
<td>SNAP</td>
<td>$12 \times 250 \text{ Msp} \text{s or } 6 \times 500 \text{ Mps} \text{s} $</td>
<td>HERA</td>
<td>$300</td>
</tr>
<tr>
<td>iTPM</td>
<td>$32 \times 1250 \text{ Msp} \text{s} $</td>
<td>AAVS1</td>
<td>$400</td>
</tr>
</tbody>
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Common problems with this approach

• Can require a node-scenario and analog signaling (e.g. HERA)
• Can require control signaling (sensors, phase switching, GPIO etc) fed back to antennas from FPGA
• Typically lots of connection points between antenna and final output signal.
• Analog artefacts such as cable reflections impact the science and result in systematics that limit the sensitivity of these low frequency instruments.
• Cross-talk between adjacent channels
Why not digitise at the antenna?

- Self-generated RFI from switching electronics and clocks
- Clock distribution over long distances
- Cost effectiveness (vs many input boards)
Self-generated RFI

- Modern Silent-Switcher-2 range DC-DC converters from Analog Devices offer excellent EMI performance
- LT8648S Step-Down converter (42V, 15A)
- >95% efficiency
- Conducted and radiated EMI at extremely low levels
- Good RFI shielding practice also helps
Timing Distribution

White Rabbit (https://white-rabbit.web.cern.ch/):

• Open Source
• Capable of synchronising 1000 nodes.
• Can work over many kilometres.
• WR products readily available off-the-shelf from several companies.
• Can be added to an FPGA platform for ~zero component cost

T.Włostowski, Precise time and frequency transfer in a White Rabbit network, 2011
https://ohwr.org/project/white-rabbit/wikis/Documents/Tom's-Master-thesis
Cost and deployment

• There are some very cheap, small FPGAs (and system-on-modules)
• Factor in extra features / cost savings:
  • Minimum signal transport costs
  • Easy antenna-control cabling
  • Lower power-dissipation / board
• Increased modularity reduces complexity
Available (low-cost) Options

• Red Pitaya
  • Cheap (from ~$250)
  • No high-speed output
  • No in-built timing recovery

• RFSoC 4x2
  • Less cheap ($2150)
  • XUP only (at this price)
  • Overkill(!)
Sparrow Project
Sparrow Project

• Includes on-board White Rabbit hardware/software for timing recovery
• Includes traditional PPS and reference inputs
• Dual inputs at 12-bits, 200-400MHz BW (ADC BW of 1.2GHz) (TI ADS5407/08/09)
• 3 x 10GbE output + White Rabbit (or 4x10 / 40GbE without WR)
• Small form-factor (only 10 x 20cm) to fit in antenna
• Compatible with a range of Xilinx Zynq chips (7-Z030/35/45)
• Potential to add mezzanine cards / analogue front-end
Sparrow Project

- Silent power solution
- 500/800/900 MSPS ADC
- 4G RAM + flash
- Xilinx ZynQ 7000 SoC (XC7Z030/35/45)
- DC, GPIO, SPI, I2C
- Dual RF inputs
- REFCLKs and Trigger
- 60-pin High speed Mezzanine connection
- WR circuits
- 3x10Gb data output + WR
- 500/800/900 MSPS ADC
- RJ45 Ethernet, USB and SD card
- 4G RAM + flash
- REFCLK, 1PPS
- 29/09/2022
First prototype and testing (XC7Z030 + ADS5407)
Completed Tasks:

• Simulink integration
• Linux image / tcpborphserver
• ADC interface
• Dual channel synchronization
• White rabbit locking
  • Huge thanks to Wei Liu
• 10 GbE support
Software pipeline

• The Sparrow SoC can host modest firmware designs but the preferred mode is one which relies on outputting synchronised ADC packets with little or no processing on the board.

• This has many advantages for astronomy F engine, FX, FXF design which can be computed on COTS server(s) and FPGA/GPU racks using widely available code.

• Writing software to turn ADC packets into e.g. a 64K channel spectrum is significantly easier and less prone to error than doing it in FPGA firmware.

• The aim is to develop Sparrow with compatible backends like GNU Radio which reduce significantly the time it takes for users to get up and running.
The short-term roadmap

• Enhance the Sparrow hardware design to enable full transceiver functionality. Our approach is to decouple TX/RX functions by not limiting our design to a particular transceiver chipset.

• Provide frequency extension from the current baseband (DC-1.2GHz) to much greater frequencies (initially up to 8GHz).

• Fine-tune the firmware needed to interface with the hardware and download data from the platform.

• Develop the primary software tools to help interface with a GNU Radio backend.
Open Source reference designs

• Our aim is to make a lot of the design files for Sparrow open-source specially daughterboards and mezzanine cards (KiCAD-6)

• Daughterboards (RF + Clocks)
  • 8GHz downconverter/downconverter
  • IQ data

• Mezzanine cards (high-speed GPIO + Clocks)
  • DAQ functionality
What Next?

• Working with Xilinx on cost minimization
• Ready to assemble rev 2
  • Minor hardware fixes
    • High bit error rate on 1 out of 4 10G interfaces
    • EOL part substitutions
• Looking for people who want to play with a board!
What Next?

Hawk?

- Zynq US+ / KU4/5P / ZU11
- 100GbE output
- AD9207 (dual chan x 6Gs/s)
- White Rabbit