USRP ‘26:
New Connections

Martin Braun

Chief RF Signal Enabler

EMERSON

Enter to Win a USRP B206mini-i!

Scan the QR code to enter for your chance to win.

NI Ettus USRP B206mini-i

No purchase necessary. One entry per person.
Winner will be selected at random and notified after the event.

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New Hardware

Pedal to the Metal

NI Ettus USRP B310

Raising the bar for entry level USRP capabilities for research, prototyping, and deployment

Applications

- Teaching and Research
- GPU Coprocessing
- Spectrum Sensing
- 5G Small Cells

Features:

- 400 MHz to 7.2 GHz frequency range
- 100 MHz Bandwidth
- 2 TX, 2 RX channel
- 2 Independent LOs
- Multi-Device-Synchronization (8x8 without external hardware)
- PCIe plug-in card or TB3 desktop module
- 10 MHz and PPS reference import, GPSDO
- GPIO, JTAG control

Benefits:

- Native GPU coprocessing via PCIe (i.e., with Nvidia Jetson)
- Available as “shielded board” for easier system integration

Thunderbolt™

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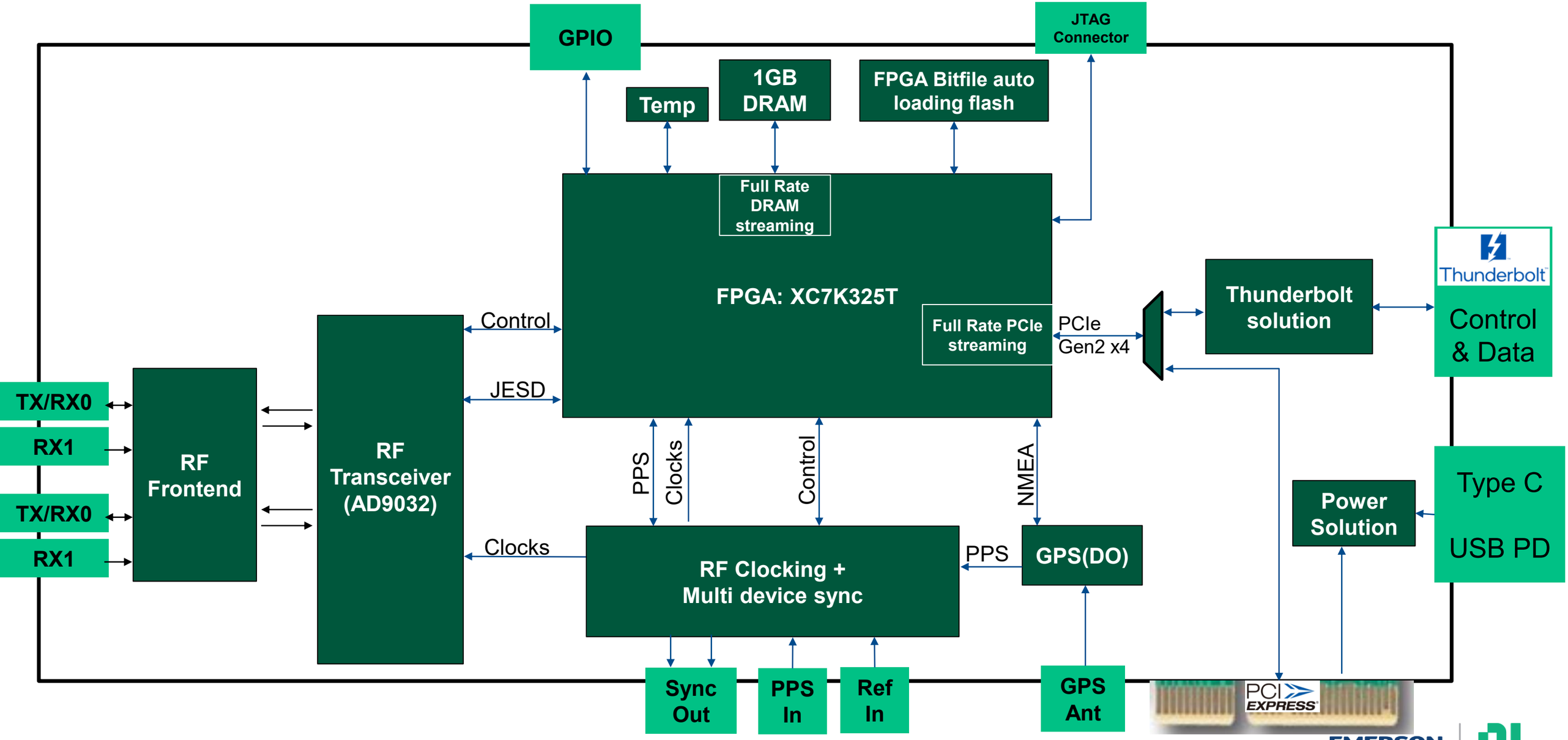
Overall Block Diagram



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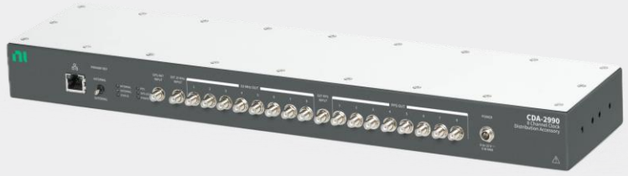
Synchronization Methods for B310

GPS-Based

- Onboard GPS Disciplined Oscillator (GPSD)
- Requires GPS antenna and GPS signal
- Scales to any number of B310s

Shared 10 MHz & PPS

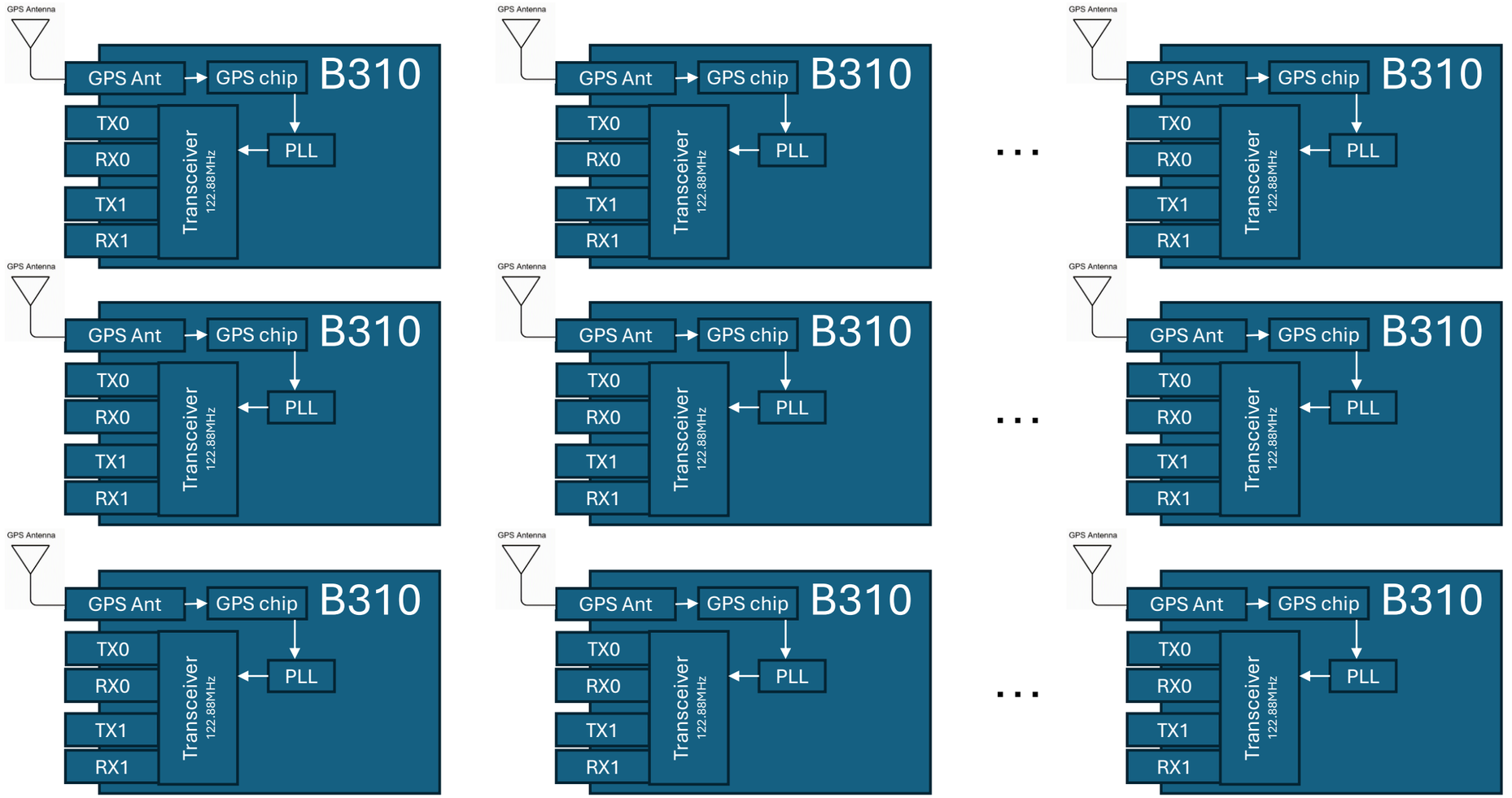
- Requires a 10 MHz and PPS signal to be provided to each B310
- CDA -2990 recommended clocking accessory
- Scales to 64+ B310s



Multi-Device

- Requires HDMI to SMA cable
- No external clocking hardware needed
- Scales to 4 B310s

GPS-Based Synchronization



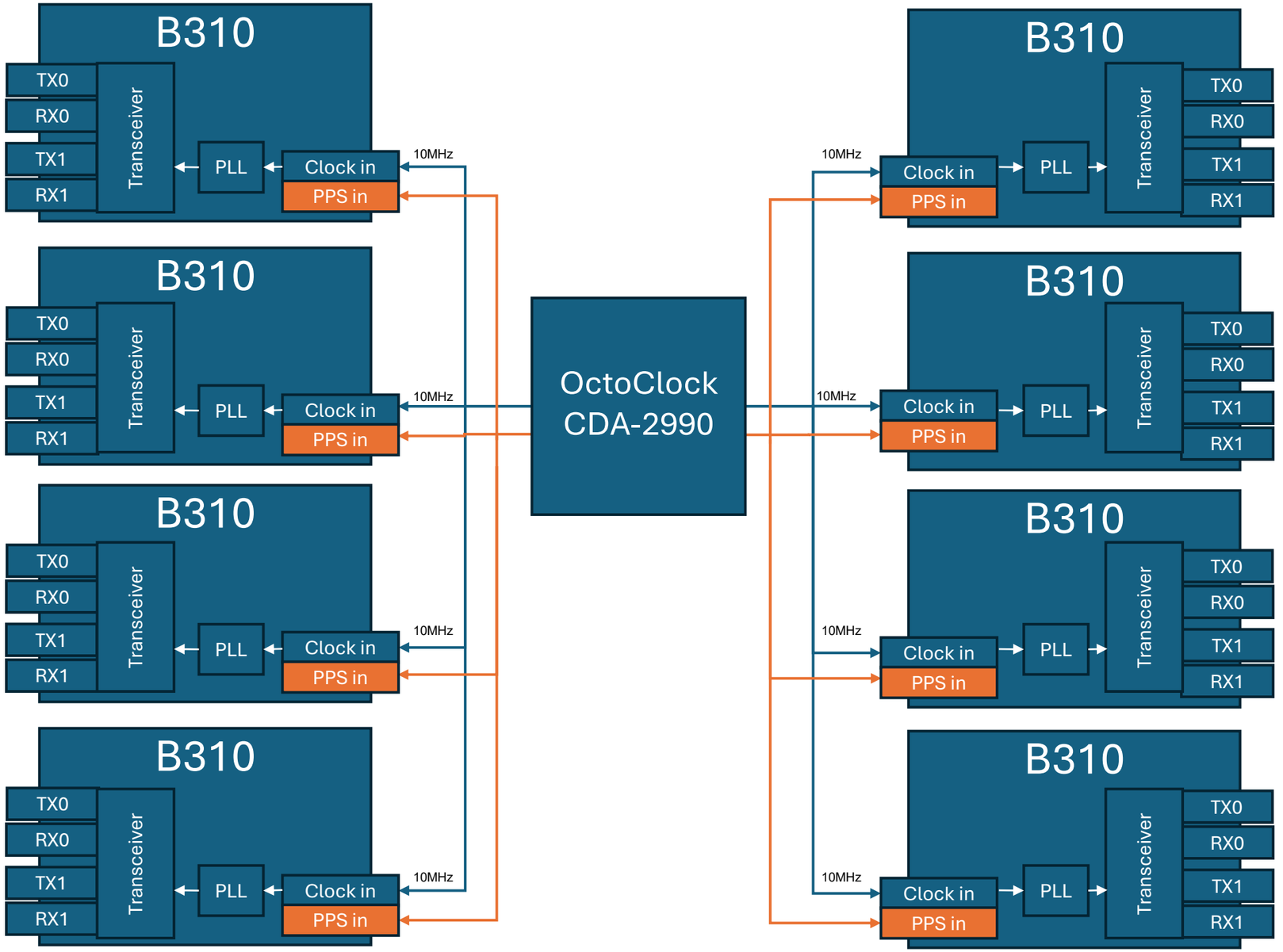
Any number of B310s with GPS antenna

x TX x RX

Freq: 350MHz to 7.225GHz

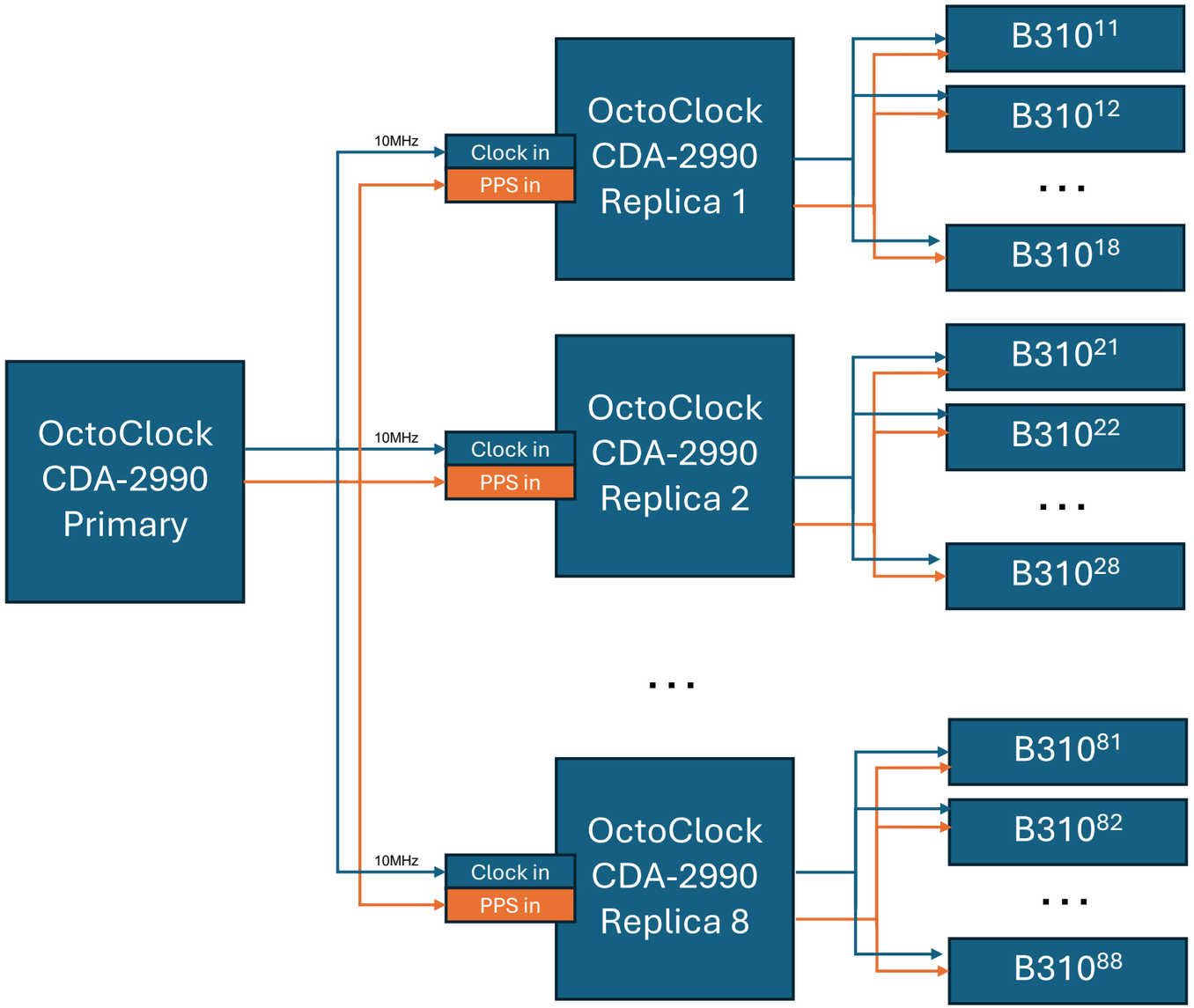
Sample Rate: 122.88MHz or 125MHz

Shared 10 MHz and PPS sync



8 B310s with one OctoClock external accessory for
16TX + 16 RX
Freq: 350MHz to 7.225GHz
Sample Rate: 122.88MHz or 125MHz
Share 10 MHz between devices for 3-10 degrees phase coherency

Shared 10 MHz and PPS sync > 16 Channel



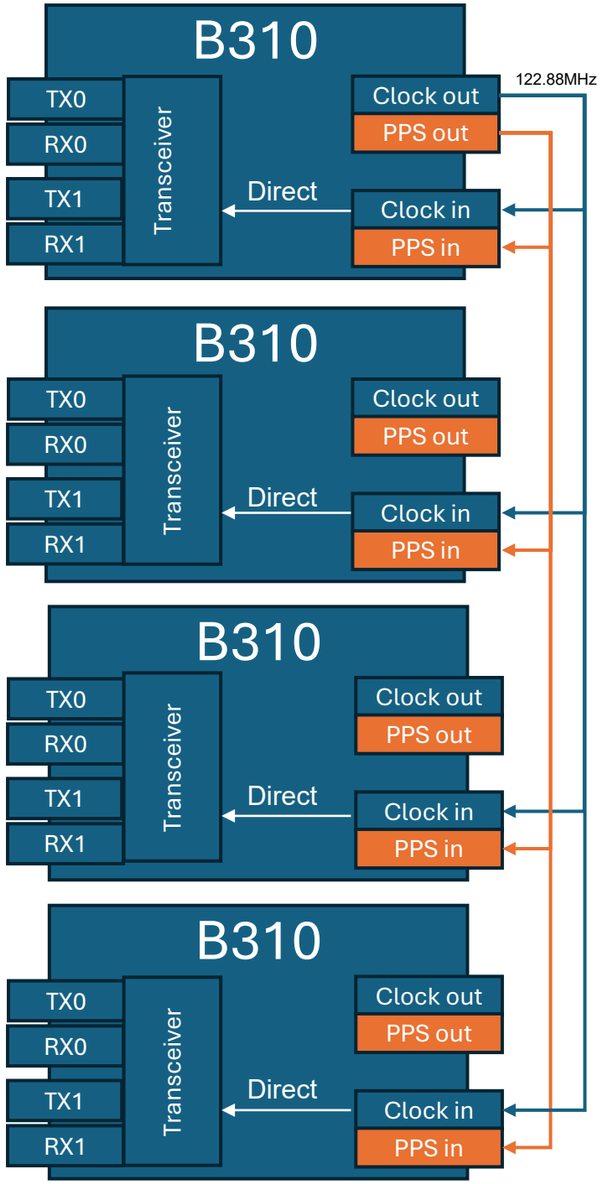
64 B310s with 9 OctoClock external accessories for

128 TX + 128 RX

Freq: 350MHz to 7.225GHz

Sample Rate: 122.88MHz or 125MHz

Multi-Device Sync



4 B310s w one Sync Cable (no external accessory needed)

8TX + 8 RX

Freq: 350MHz to 7.225GHz

Sample Rate: 122.88MHz or 125MHz

Share ref clock directly for 1-2 degrees phase coherency

NI Ettus USRP X420

Research and Prototyping in 5G NR FR3 and X-/Ku-band multi-channel applications

Applications

- Radar/EMSO
- Satellite communications
- Non-terrestrial networks (NTN)
- 6G research in FR3

Features:

- 10 MHz to 20 GHz frequency range
- Up to 1 GHz Bandwidth
- 2 TX, 2 RX channel
- Multi-Channel Phase Coherency <1 degree RMS
- 5G NR RX EVM of < -35 dB at 7 GHz
- Xilinx Zynq Ultrascale+ RFSoC ZU28DR
- Dual 100 Gigabit Ethernet or Aurora via QSFP28
- 10 MHz and PPS reference import, LO export and import per channel
- GPIO, JTAG control
- UHD / RFNoC as you know it!

Benefits:

- Expanding USRP frequency range to 20 GHz for applications like multi-channel radar systems and NTN for 6G
- Highest quality RF performance USRP ever released

X420 – Connectivity

RF: 2x2, 10 MHz – 20 GHz + LO sharing

GPIO

Streaming: Dual 100 GbE

Power & Management

Timing: GPS, 10 MHz, PPS

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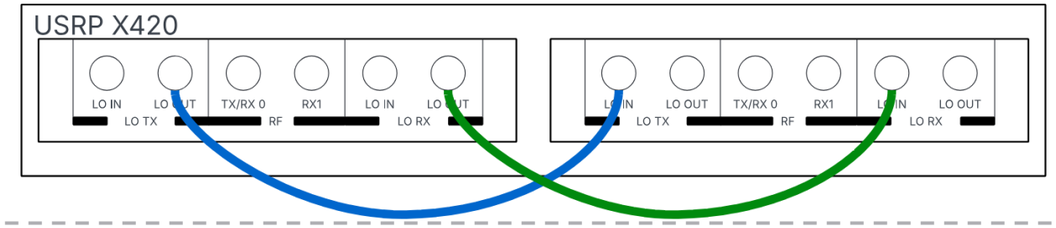
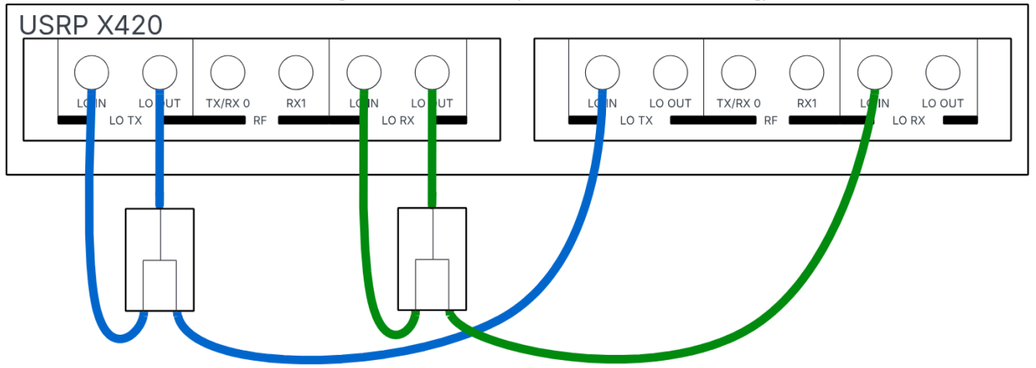
X420 – LO Sharing Flexibility

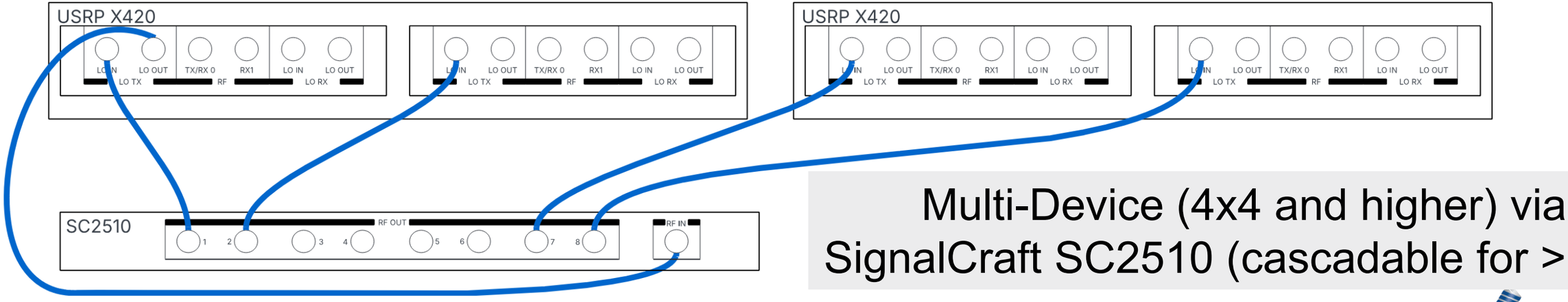
USRP Hardware Driver and Device Manual: HBX Daughterboard



Simple 2x2 coherent system



Recommended 2x2 coherent system (symmetric using passive splitter)

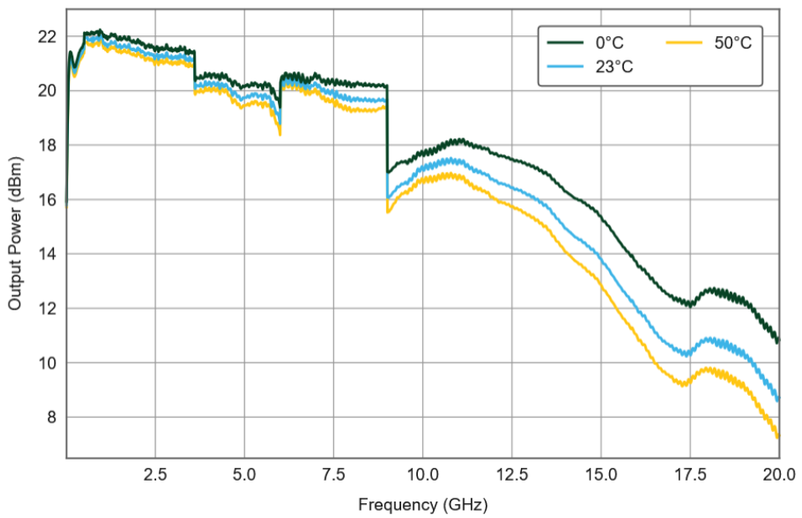


Multi-Device (4x4 and higher) via SignalCraft SC2510 (cascadable for > 8x8)

Ettus USRP X420 Specifications

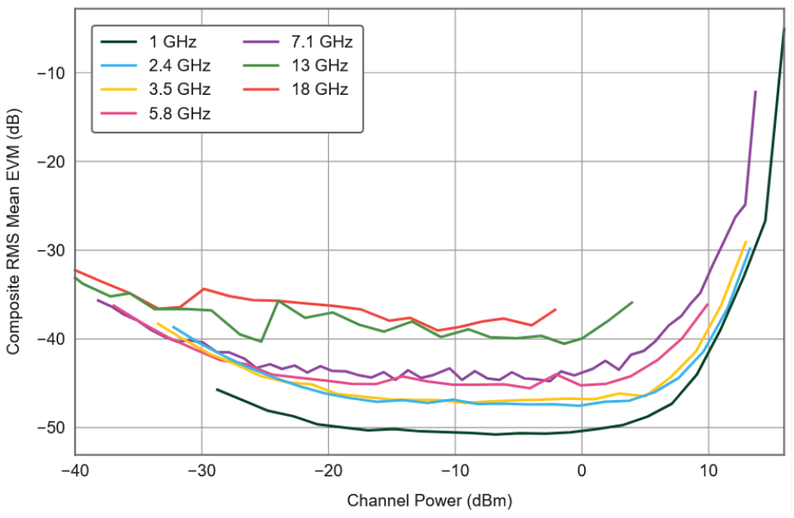
X420 Specification Highlights

TX output power over temp

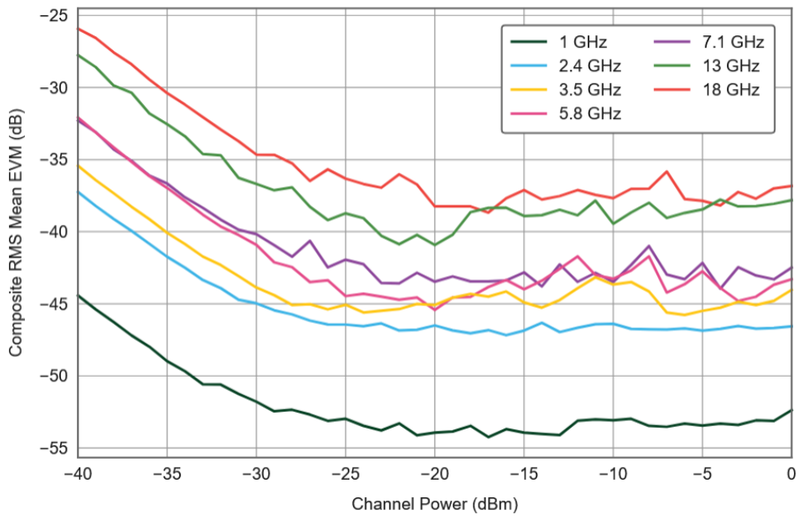


Power of CW tone, TX at max gain.

EVM Bathtub TX



EVM Bathtub RX



Internal LO, IQ corrections applied, at center frequency
5G NR, 400 MHz BW, SCS 120kHz, 256 QAM

Much more content on the specifications page!

Ettus USRP X420 Specifications

X420 Specification on Phase Coherency

Using LO Sharing / Reference Sharing (Octoclock + SC2510)
[see spec page for more details]

TX Phase Stability

Table 42. TX Phase Stability (Standard Deviation)

Tune Frequency	Single Device Phase RMS	Single Device Delay RMS	Multi-Device Phase RMS	Multi-Device Delay RMS
2.4 GHz	0.082 deg	0.206 ps	0.150 deg	0.824 ps
5.8 GHz	0.031 deg	0.206 ps	0.045 deg	0.824 ps
10 GHz	0.040 deg	0.206 ps	0.072 deg	0.824 ps
13 GHz	0.038 deg	0.206 ps	0.075 deg	0.824 ps
18 GHz	0.045 deg	0.206 ps	0.093 deg	0.824 ps

RX Phase Stability

Table 43. RX Phase Stability (Standard Deviation)

Tune Frequency	Single Device Phase RMS	Single Device Delay RMS	Multi-Device Phase RMS	Multi-Device Delay RMS
2.4 GHz	0.010 deg	0.092 ps	0.029 deg	0.666 ps
5.8 GHz	0.003 deg	0.092 ps	0.006 deg	0.666 ps
10 GHz	0.017 deg	0.092 ps	0.043 deg	0.666 ps
13 GHz	0.016 deg	0.092 ps	0.054 deg	0.666 ps
18 GHz	0.038 deg	0.092 ps	0.073 deg	0.666 ps

TX Phase Repeatability

Table 44. TX Phase Repeatability (Power-Cycle Events)

Tune Frequency	Single Device Phase RMS	Single Device Delay RMS	Multi-Device Phase RMS	Multi-Device Delay RMS
2.4 GHz	0.016 deg	0.119 ps	0.280 deg	4.514 ps
5.8 GHz	0.048 deg	0.119 ps	0.106 deg	4.514 ps
10 GHz	0.066 deg	0.119 ps	0.141 deg	4.514 ps
13 GHz	0.072 deg	0.119 ps	0.202 deg	4.514 ps
18 GHz	0.087 deg	0.119 ps	0.239 deg	4.514 ps

RX Phase Repeatability

Table 45. RX Phase Repeatability (Power-Cycle Events)

Tune Frequency	Single Device Phase RMS	Single Device Delay RMS	Multi-Device Phase RMS	Multi-Device Delay RMS
2.4 GHz	0.002 deg	0.083 ps	0.011 deg	3.888 ps
5.8 GHz	0.005 deg	0.083 ps	0.012 deg	3.888 ps
10 GHz	0.011 deg	0.083 ps	0.030 deg	3.888 ps
13 GHz	0.013 deg	0.083 ps	0.039 deg	3.888 ps
18 GHz	0.013 deg	0.083 ps	0.021 deg	3.888 ps

The most coherent USRP we ever specified!

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USRP Product Portfolio Overview

Ettus USRP B2XX	Ettus USRP E320	Ettus USRP N310 / N32X	Ettus USRP X310	Ettus USRP X410	Ettus USRP X440	Ettus USRP X420
Entry Level (up to 100MHz / channel, SWAP optimized, <$10k)		Mid-Range (up to 200MHz / channel, onboard FPGA DSP, flexible configurations, $10-25k)		High-End (up to 1.6GHz/channel, large FPGA capacity, $25-50k)		

Recent additions

B206mini-i

Small form factor
Entry level pricing
1x1, 56MHz, 6GHz

B310

TB3, PCIe or board only
GPU coprocessing
2x2, 100MHz, 7.2GHz

OBX-160

X310/X300 compatible
Up to 8.4 GHz frequency range
2x2 (per X310), 160MHz, 8.4 GHz

X420

Highest end USRP
Phase coherency
2x2, 1 GHz, 20GHz

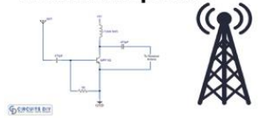
Let us know if your solution shall be listed on ettus.com

The USRP Ecosystem

Frontends & HW Accessories

...& more + DIY

Antenna Amplifier



Toolflow Support

Comms Stack Integration

System Integration

New Software

As in, Software Defined Radio

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2 Releases since GRCon ‘25

- Every new hardware comes with a new release: 4.10 brought X420, 4.11 brought B310
- Approximate 6-month UHD release cycle has been stable for a while now
- We’ve been good boy scouts about making better and more useful release notes

- Installers typically come with a slight delay
  - Now includes ARM64 installers for Ubuntu!

- Every release comes with brand new features, but we do spend a lot of time fixing bugs (even on old devices!)
  - Check the release notes, there might be something for your device and/or use case!

UHD-4.11.0.0

UHD 4.11.0.0 Release

- Highlights / Main Changes
  - Add support for the new USRP B310, a PCIe/Thunderbolt-based device which supports 2x2 RF channels at up to 100 MHz bandwidth per channel.
  - Update underlying OE version on embedded devices to Scarthgap (5.0 LTS). Note that some of the MPM updates require this update.
  - Migrated the MPM RPC transport layer from mprpc (msgpack-RPC) to gRPC/Protobuf, impacting all embedded devices running MPM.
- New Features
  - X440:
    - The X440_X4_200 image now uses fabric resamplers instead of RFDC

UHD 4.10.0.0 Latest

fdietze-ni released this Apr 27 · 369 commits to master since this release v4.10.0.0 2af4ddb

UHD 4.10.0.0 Release

- Highlights / Main Changes
  - Support for USRP X420
  - Addition of timed complex gain feature, which allows setting a complex gain value to fix phase and amplitude of signals from radio blocks
- New Features
  - CMake:
    - Create UHD::uhd package for improved integration in downstream build processes. The init_usrp example is used to showcase this feature.
    - Improved options for RFNoC OOT modules to write unit tests.
  - Add helper routines to up- and download data (reliably) from and to the

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Timed Gain and Phase Control

- **Change gain and phase per channel** for transmit and receive signals
  - $y[n] = x[n] \cdot \boldsymbol{g} \cdot e^{j\boldsymbol{\phi}}$
  - Included into most shipping bitfiles USRPs {X3xx, N3xx, X4xx}
  - Use with Multi-USRP and RFNoC APIs
  - Timed and non-timed control options

- **Example applications**
  - Enables multi-channel phase and amplitude calibration
  - Digital beam steering

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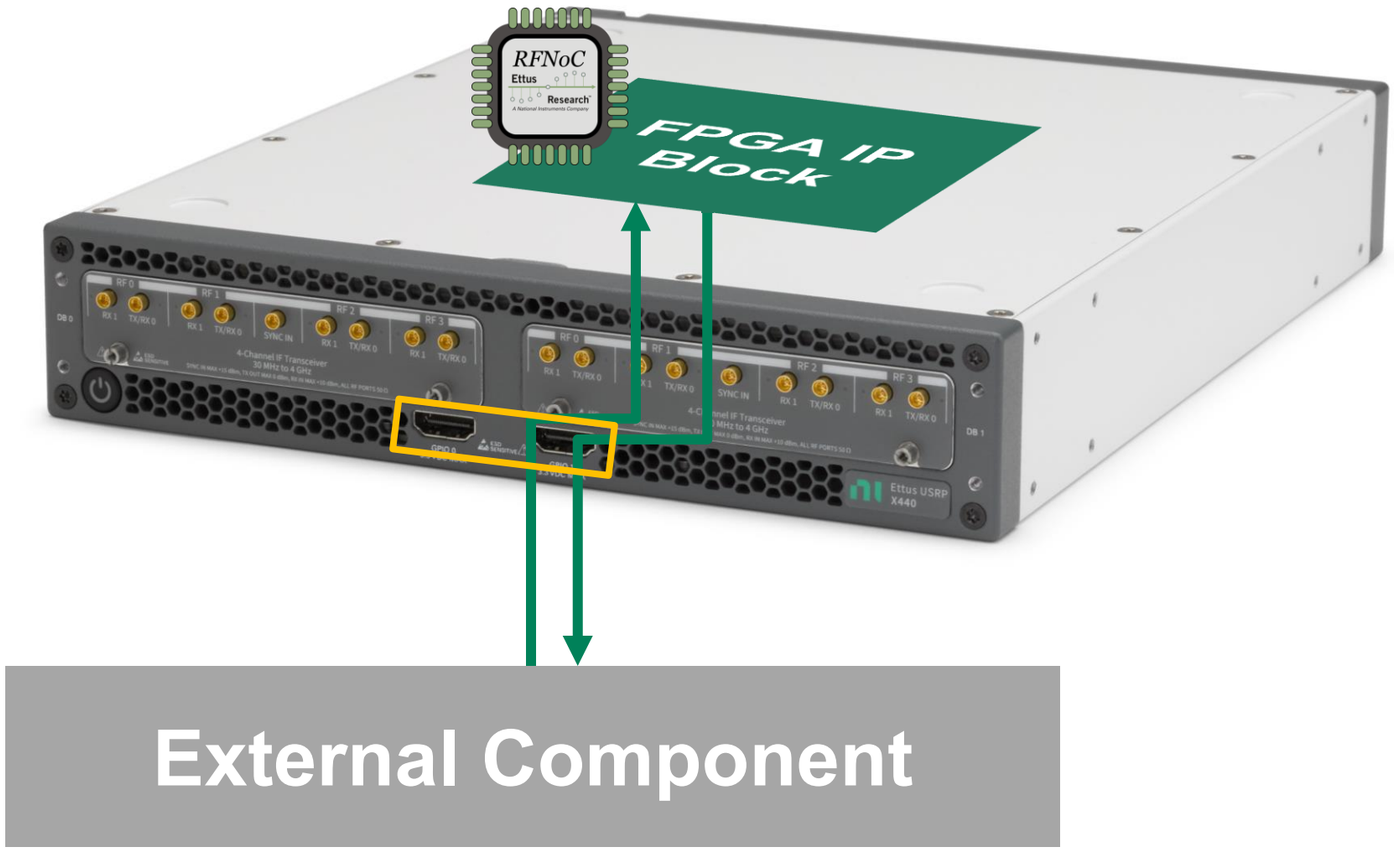
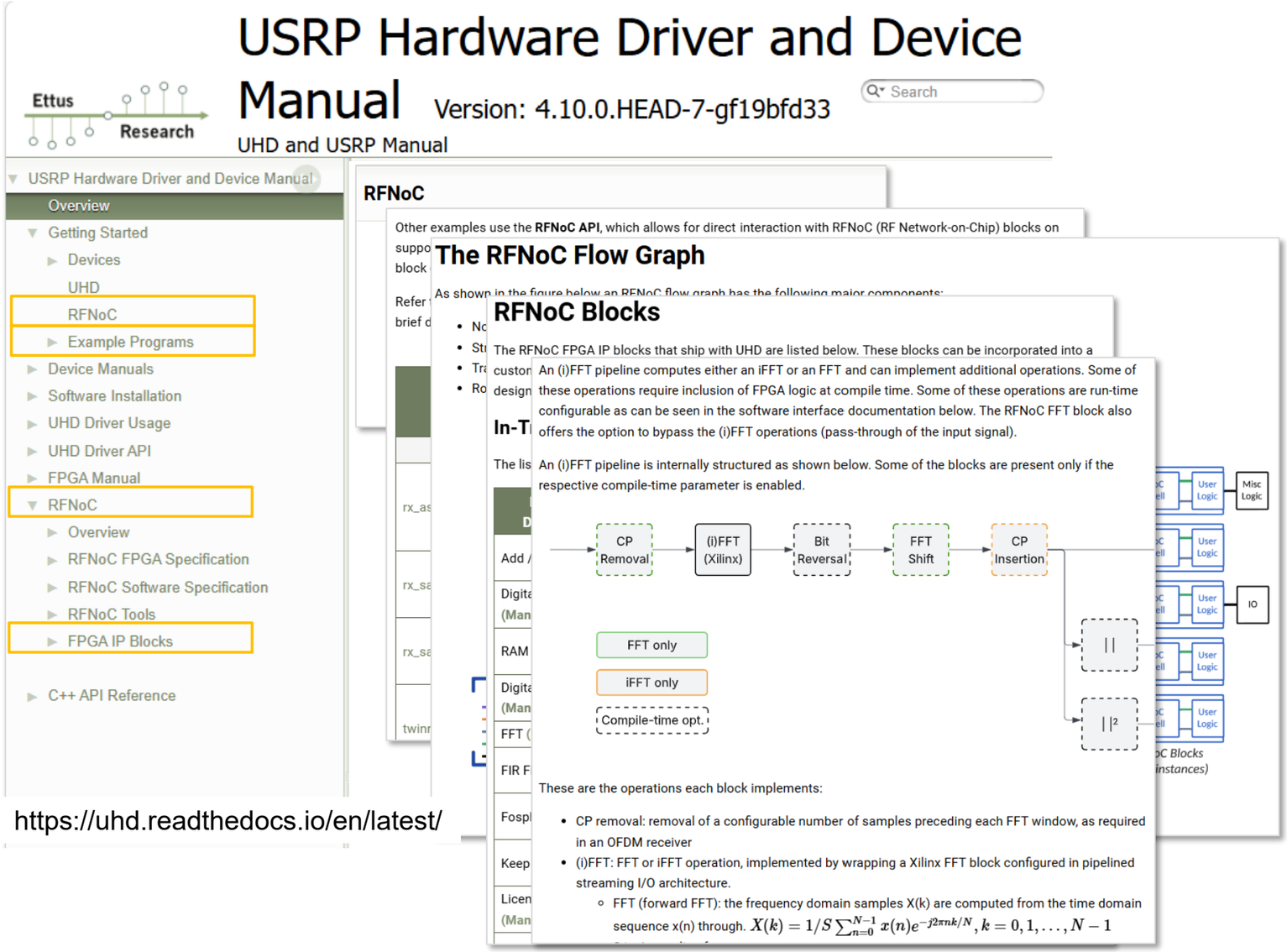
Accessing GPIO from RFNoC FPGA IP Blocks



- **GPIO use before UHD 4.10**
  - Toggle GPIO lines automatically to reflect transmit and receive states
  - Drive GPIO lines from host software (slow)
  - X4xx – SPI commands (fast)
- **Added in UHD 4.10**
  - Connect arbitrary GPIO lines to a custom RFNoC FPGA IP block
  - Control external components from the FPGA
  - Control FPGA processing based on externally provided signals
  - Works with all USRPs supporting RFNoC

Improved UHD Manual and Examples



https://uhd.readthedocs.io/en/latest/

In-code help in all UHD examples

```
rfnoc_replay_samples_from_file_help.txt
usage: rfnoc_replay_samples_from_file [-h] [--args ARGS] -f FREQ -r RATE
                                       [--tx-args TX_ARGS]
                                       [--radio-id RADIO_ID]
                                       [--radio-chan RADIO_CHAN]
                                       [--replay-id REPLAY_ID]
                                       [--replay-chan REPLAY_CHAN]
                                       [--nsamps NSAMPS] [--file FILE]
                                       [--lo-offset LO_OFFSET]
                                       [--gain GAIN] [--ant ANT]
                                       [--bw BW]
                                       [--ref {internal,external,mimo,gpsdo}]
                                       [--dot]

This example program demonstrates how to use the RFNoC C++ API
to create an RFNoC graph involving an RFNoC Replay block for playback of
baseband samples through the radio.
The program loads sample data into the Replay block, configures the RF
chain, and plays back the data through the radio. Playback can be
continuous or for a specified number of samples.

Notes:
  - The Replay block is included in most default FPGA images for
    RFNoC-capable USRP devices, so custom FPGA builds are usually not
    required to use this example program.
  - The USRP may round the requested transmit sample rate to the nearest
    supported value. For accurate playback, please ensure that the sample
    rate of the input data in the file matches the USRP sample rate.
    If supported by your USRP device model, you could also change the
    master clock rate to an integer multiple of the desired sample rate
    to achieve precise sampling. For available master clock rates for a
    specific USRP device model, see the UHD manual.

Key features:
- Loads baseband samples from a binary file and uploads them to the
  RFNoC Replay block for playback through the radio.
- Dynamically builds and configures an RFNoC graph connecting the Replay
  block to the radio block, with automatic integration of a DUC block if
  present.
- Supports flexible selection of Replay and radio blocks and channels
  via program options.
- Allows configuration of key transmission parameters, including
  frequency, sample rate, gain, bandwidth, LO offset, and antenna.
- Enables continuous or finite playback of samples, as specified by the
```

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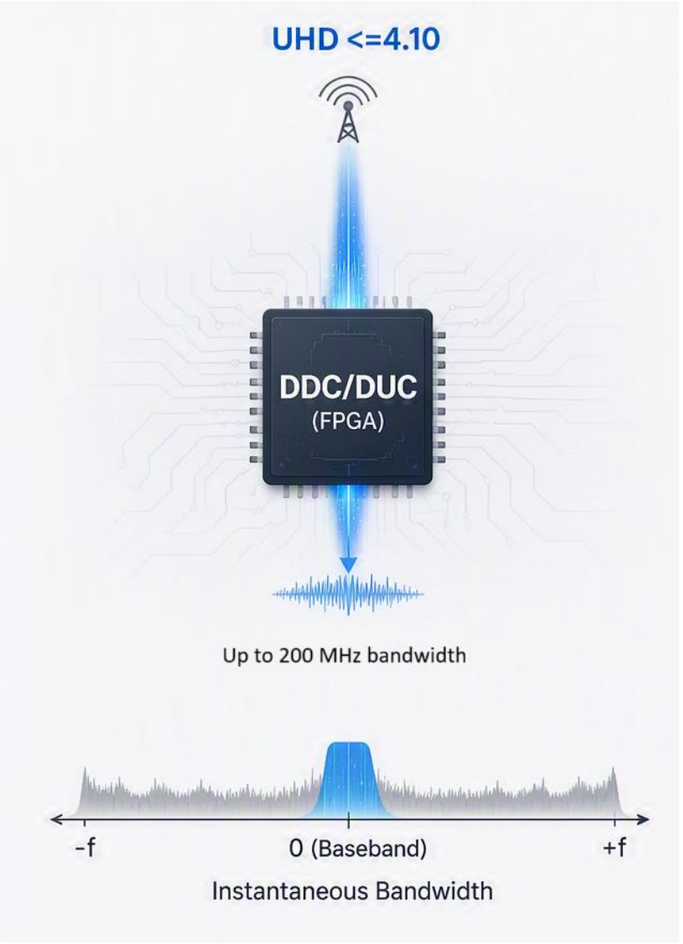
Wideband DDC and DUC



UHD ≤4.10

- DDC/DUC only up to 200 MHz
- No integration into FPGA images with higher bandwidth

Starting with UHD 4.11

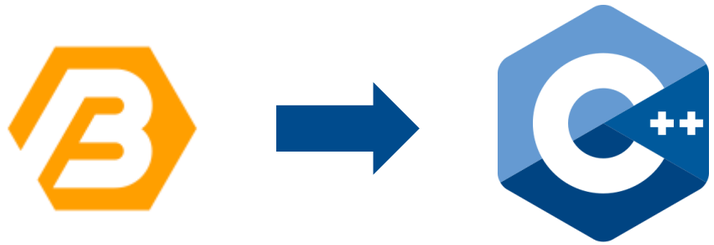
- Wideband DDC/DUC blocks for up to 1600 MHz
- Integrated into most X4xx FPGA images:
  - x410_X4_400,
  - x410_CG_400,
  - x420_X4_1000,
  - x420_CG_1000,
  - x440_X4_1600,
  - x440_CG_1600
- Integration into own designs possible

- More rate variability:
  - Change sample rate within UHD session,
  - pick small subbands from large bandwidth

Modernization

Investments into keeping our platform up-to-date and safe:

- Message Pack RPC ➔ gRPC with protobuf for the control communication between UHD host and embedded devices like X4xx or N3xx (New dependencies!)
- Embedded OS updated to Yocto Scarthgap (5.0 LTS) and Linux kernel 6.12 for all our embedded devices
- Replaced (some) Boost dependencies with newer C++ equivalents
  - Faster compilation, less dependencies, more useful error messages when compiling UHD yourself
- Moving to C++20 for the library
- Yes, we're aware of the CRA



More RFNoC Improvements!

- Implemented RFNoC protocol version 2:
  - Block operations, burst operations, polling
  - Provides improved handling of lossy networks
- Improved FPGA resource utilization
- VHDL 2008 support
- …and so on

Control packet field usage.

OpCode	Operation	Request Data	Response Data	Description
0	Sleep	NumData = 1 Data[0] = Stall cycles	NumData = 0 No data words are included in the response.	Do nothing and stall the control endpoint for *Data*[0] clock cycles of the control interface clock.
1	Write	NumData = Number of data words to write (1 to 15) Data[0] = Value of first word to write ... Data[*NumData*-1] = Value of last word to write	NumData = 0 No data words are included in the response.	Write *Data*[*n*] to a single *Address* at all bytes *p* where *ByteEnable*[*p*] = 1.
2	Read	ReqSize = Number of data words to read (1 to 15) NumData = 0 No data words are included in the request.	NumData = Number of data words in response Data[0] = Value of first word read ... Data[*NumData*-1] = Value of last word read	Read *ReqSize* times from *Address*. The response contains each read result in *Data*[*n*].
3	Read then Write	NumData = 1 Data[0] = Value of data word to write	NumData = 1 Data[0] = Value of data word read	Read a data word from *Address*, then write a data word to it at all bytes *p* where *ByteEnable*[*p*] = 1.
4	Block Write	NumData = Number of data words to write (1 to 15) Data[0] = Value of first word to write ... Data[*NumData*-1] = Value of last word to write	NumData = 0 No data words are included in the response.	Write *Data*[*n*] to registers sequentially at (*Address* + 4·*n*) at all bytes *p* where *ByteEnable*[*p*] = 1, for n = 0 .. *NumData*-1.
5	Block Read	ReqSize = Number of data words to read (1 to 15) NumData = 0 No data words are included in the request.	NumData = Number of data words in the response Data[0] = Value of first word read ... Data[*NumData*-1] = Value of last word read	Read *ReqSize* registers sequentially starting at *Address*, incrementing by 4 each step (*Address* + 4·*n*, n = 0 .. *ReqSize*-1). The response contains the register values in Data[0]..Data[*NumData*-1].
6	Poll	NumData = 3 Data[0] = Data Data[1] = Mask Data[2] = Timeout	NumData = 1 Data[0] = Value of the last data word read	Poll on *Address* until its value for all bits in *Mask* matches *Data* & *Mask*, or until *Timeout* cycles of control interface clock have elapsed. The response contains the last value of *Data* that was read. Acknowledged with CMDERR if timeout occurs, otherwise with OKAY.
7-9	Reserved	Reserved	Reserved	Reserved
10-15	User Defined	User Defined	User Defined	These opcodes are reserved for user-specific implementation.

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RFNoC Shop Competition

Win a brand new USRP B310!

1) Submit a block to the NoC Shop by 03/10/27
2) The NI team will pick blocks in 2 categories:
   - Most creative block
   - Most impactful contribution
3) The top two winners will get a USRP B310!

Learn more

It’s that simple. Submit your block today

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There’s more…

- …but no more time

- Check out release notes or ask us!

Thank You!

…for being at GRCon, and being part of this community
…for listening to me talk, and visiting our booth
…for being part of the USRP ecosystem

UHD Simulator

Auto-Rx-on-Tx

CMake
UHD::uhd
package

Holoscan
Example (GPU
Processing)

…

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NI Ettus USRP B206mini-i

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