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RadioStream: A Wideband Multi-Antenna SDR Platform

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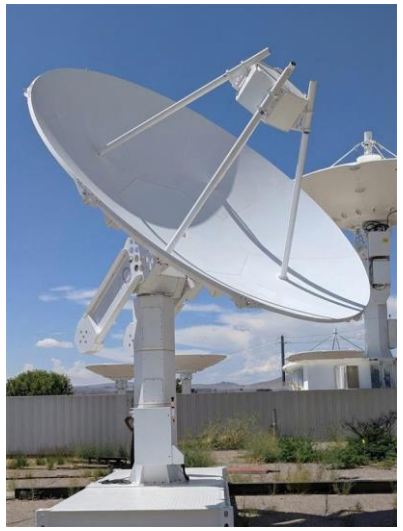
SDRs in wireless communication

Cellular Infrastructure

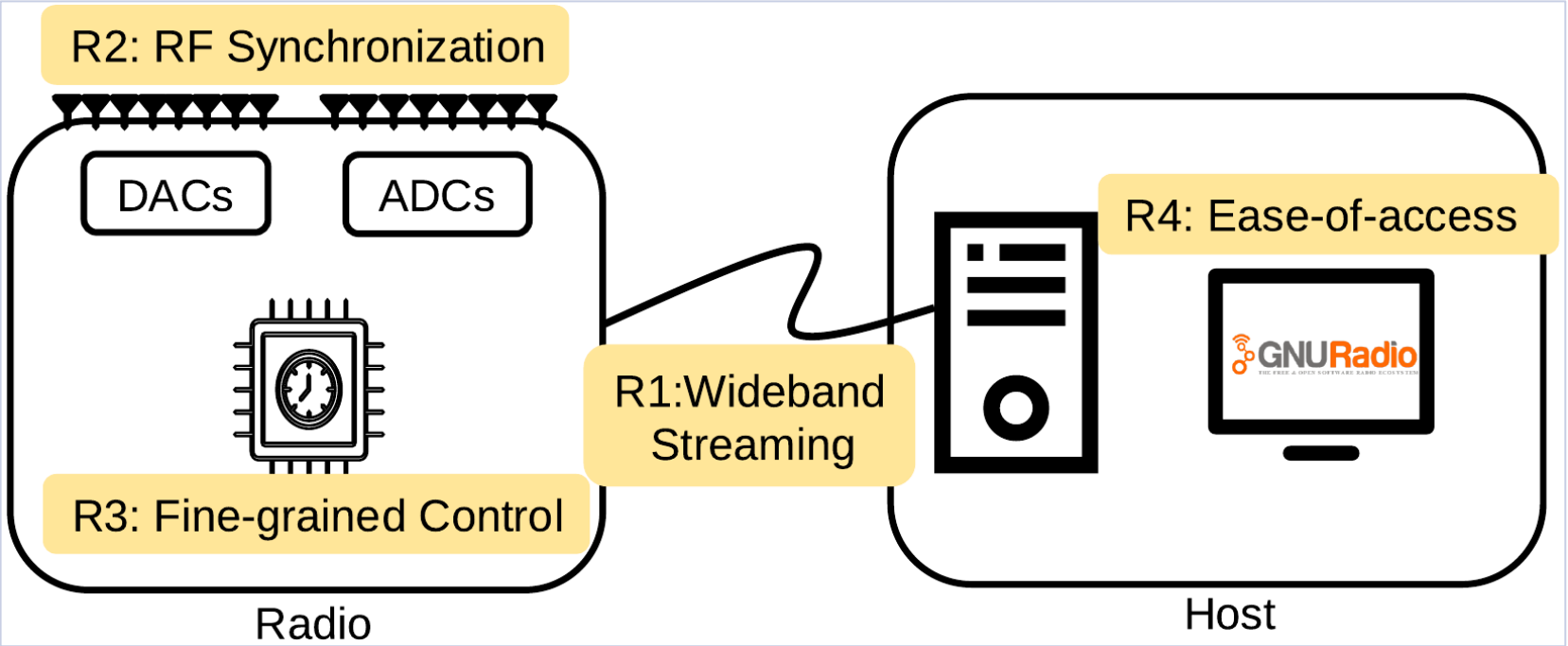
Military and Defence



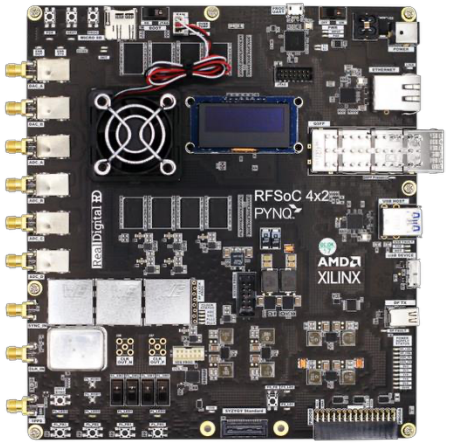
Space Communications

Surveillance

Four key requirements for building an SDR



- **R1** Wideband streaming
- **R2** RF synchronisation
- **R3** Fine-grained control
- **R4** Ease of access



Where the Us and Os come from in UHD based SDRs

UUU OOOOOO L UUUUU OOOOOOOO LL UUUU OOOOO

RADIO (FPGA + RF front-end)

- **Deterministic and Clock driven**
- Locked to the RF sampling clock
- Keeps exact time, but limited to shallow on-chip SRAM FIFOs (≤ 1 MB)

≠

two clocks, one timeline

HOST (x86 + Linux)

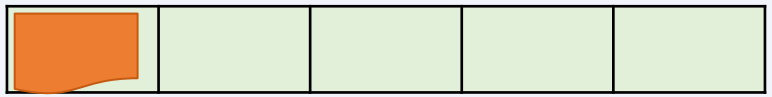
- **Non-deterministic and Software driven**
- OS scheduling, interrupts, queueing
- Has massive compute capacity, but transmission timing is highly variable

U – Underflow, O – Overflow, L – Late Packet

Issues with host centric systems

RADIO (FPGA + RF front-end)

Buffers:



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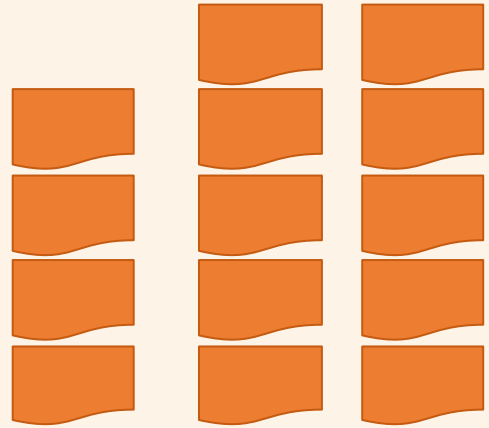
HOST (x86 + Linux)



Host-centric systems → Deploy buffer flow control mechanisms → Loop: feedback messages from FPGA -> Host transmissions (tight boundary) → Even a very small context switch in the host -> Underflow

FLIP THE SWITCH: FPGA drives the data streaming

1
FPGA owns time

A counter running on the RF sampling clock generates a tick every 0.5 ms [defined as a **SLOT**]

Generates a tick with SLOT NUMBER every 0.5 ms

2
Host programs the future

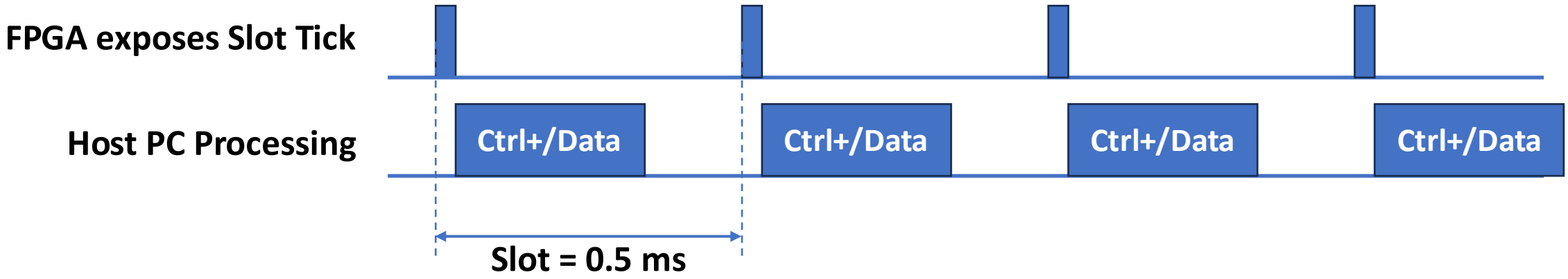
On reception of tick, it sends configuration and/or samples labelled for the upcoming slot.

two-slot look-ahead

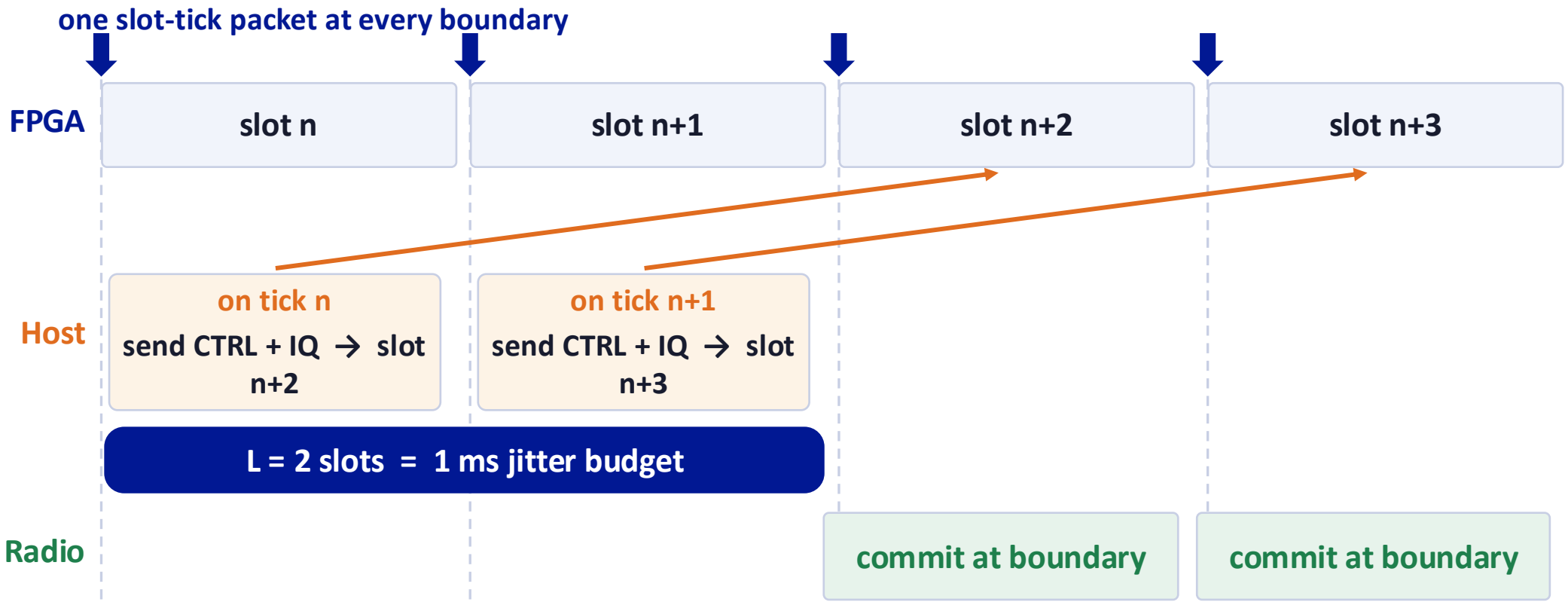
3
FPGA commits at the boundary

IQ samples are held in a buffer, transferred only when the counter reaches that slot.

slot-indexed PL-DDR4 buffers



System timing: Two slots look-ahead, commits at the boundary

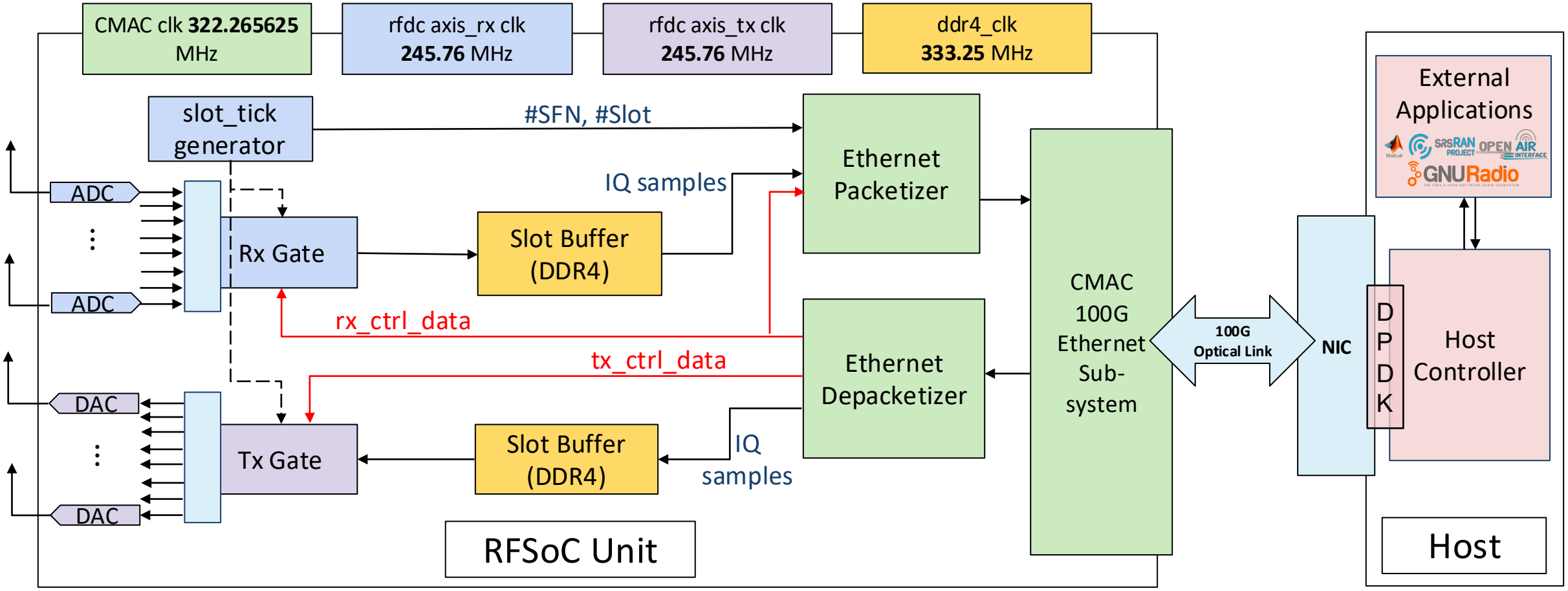


Slot-aligned elastic buffering

≥ 4 slots in PL-DDR4 (2 uplink + 2 downlink) - about 64 Mb for 8 channels at 122.88 MHz, too large for BRAM or URAM.

The host never races a deadline - it labels its intent, and the FPGA decides when that intent becomes real.

RadioStream architecture



RFSoC - data plane

ADC -> rx_gate -> DDR4 slot buffer -> packetizer

RFSoC - timing

slot_tick_generator drives both the gates and commit to host

Host

DPDK owns the fronthaul; shared memory feeds Application

Receiving samples at the host

Current SDRs: UHD + DPDK

NIC -> DPDK Poll -> UHD/CHDR Parse -> Application

√ Kernel bypassed entirely; user-space polling

√ CPU crushed by closed-loop CHDR buffer - flow control (ACKs) and iterative, per-sample format unpacking

√ A single OS scheduler pause starves the tiny FPGA SRAM buffer

RadioStream: DPDK + Shared Mem

NIC -> DPDK Poll -> Pointer ring -> rte_memcpy -> shared Mem -> Application

√ Zero kernel copies, zero syscalls

√ Single, vectorized user-space block copy

√ Lockless atomic handoff with Shared Mem Ring

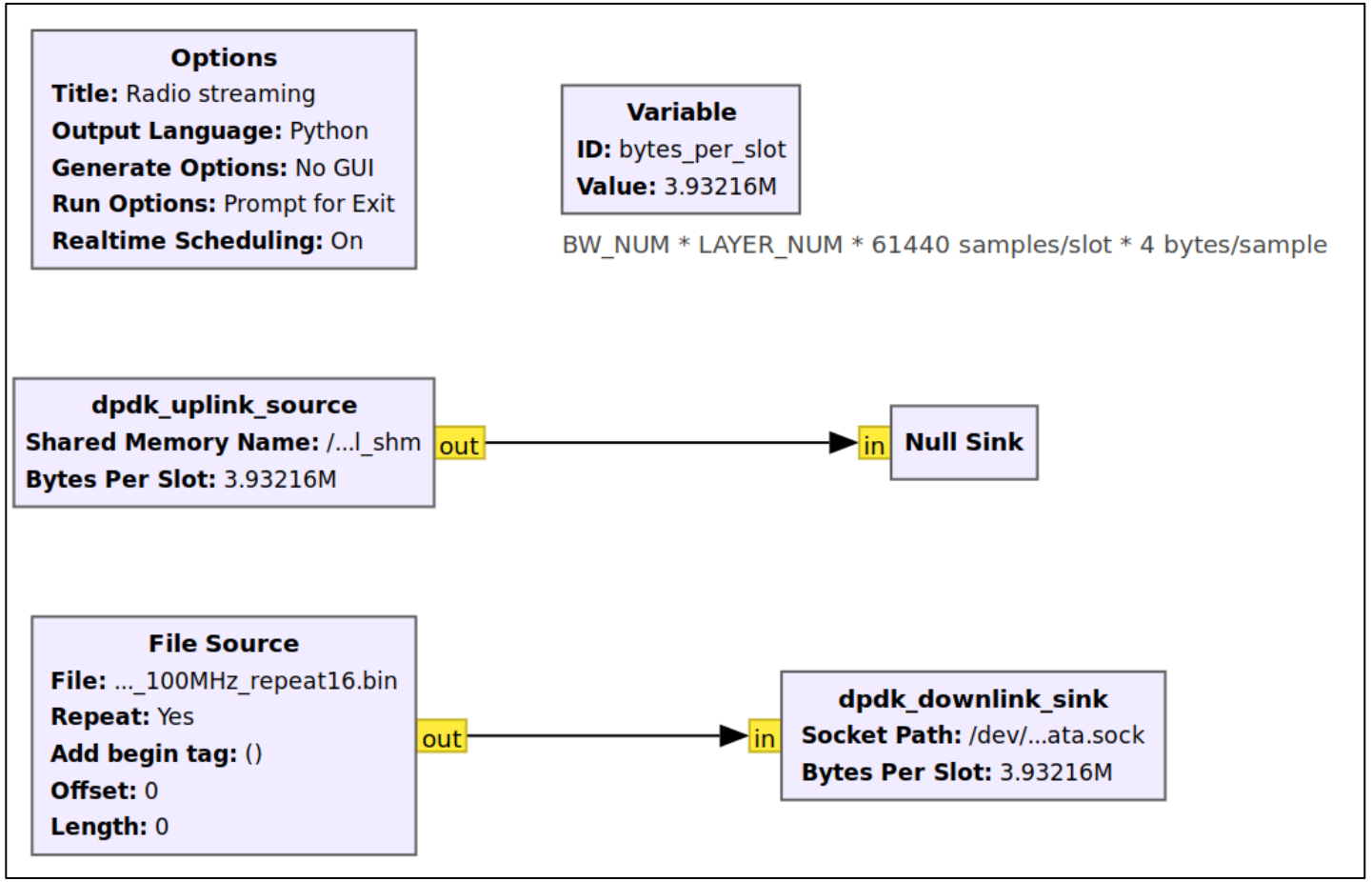
√ Fully saturates 98 Gbps using exactly 3 CPU cores

GNU Radio integration

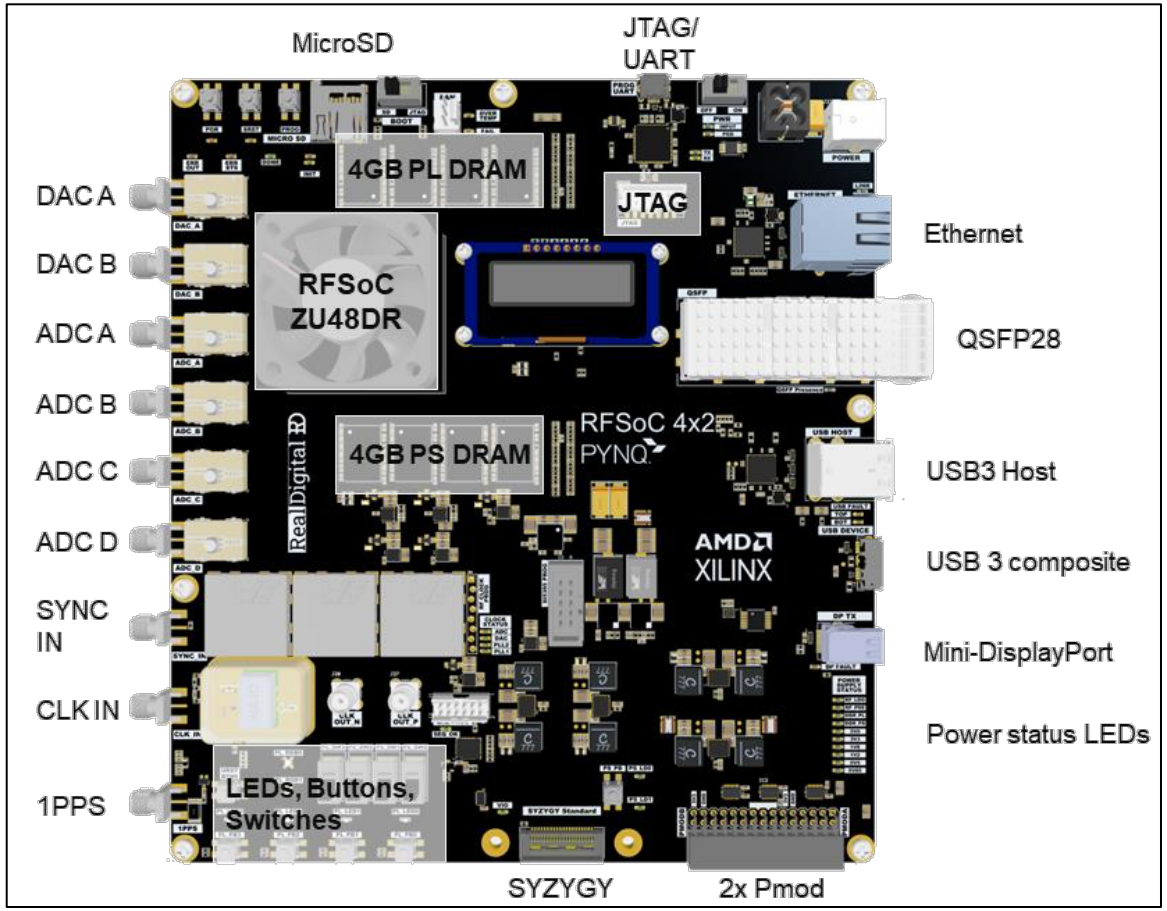
1. **Zero-copy OOT blocks:** dpdk_uplink_source and dpdk_downlink_sink map the shared-memory ring directly.

2. **No DPDK dependency in GNU Radio:** GNU Radio links standard C++ shared memory; only the host controller links DPDK.

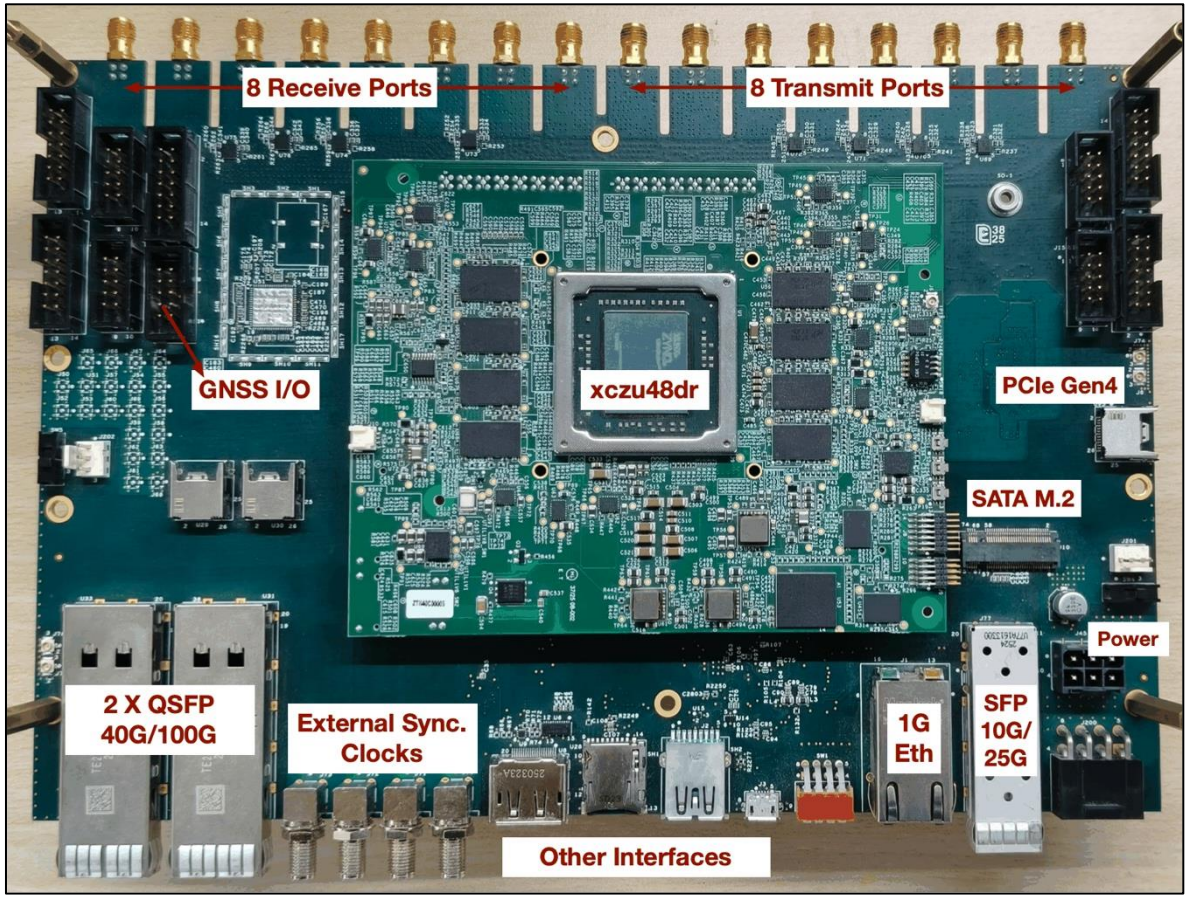
3. **Independent pipelines:** GNU Radio scheduler stalls do not perturb the fronthaul transport.



Implementation



(a)



(b*)

Implemented and tested the design on **(a)** RFSoC 4x2 (4 ADC / 2 DAC) and **(b)** a custom 8T8R SOM, both XCZU48DR. Host is verified with both Mellanox ConnectX-5 and Intel E810 - the result reproduces on both.

*The custom SOM + RF Carrier boards are developed by REIO Systems Pvt. Ltd., India

Throughput and transport latency

transport time for one slot (µs) / instantaneous throughput (Gbps), 1-hour average.
orange = limited by the memory path, not the 100G link

BW	Path	1 ch	2 ch	4 ch	8 ch
122.88 MHz	FPGA ↔ Host	19.98 / 98.4	39.82 / 98.8	79.60 / 98.8	159.3 / 98.7
	Host ↔ App	15.11 / 130	30.09 / 131	59.88 / 131	120.2 / 131
245.76 MHz	FPGA ↔ Host	39.81 / 98.8	79.59 / 98.8	159.3 / 98.8	346.6 / 90.8
	Host ↔ App	29.97 / 131	59.81 / 131	120.4 / 131	294.1 / 107
491.52 MHz	FPGA ↔ Host	79.59 / 98.8	159.3 / 98.7	345.7 / 91.0	-
	Host ↔ App	59.88 / 131	120.2 / 131	295.8 / 106	-

~2 GHz
max aggregate RF BW

90-100 Gbps
sustained on the link

0
drops in 1 hour testing

3 cores
in the host controller

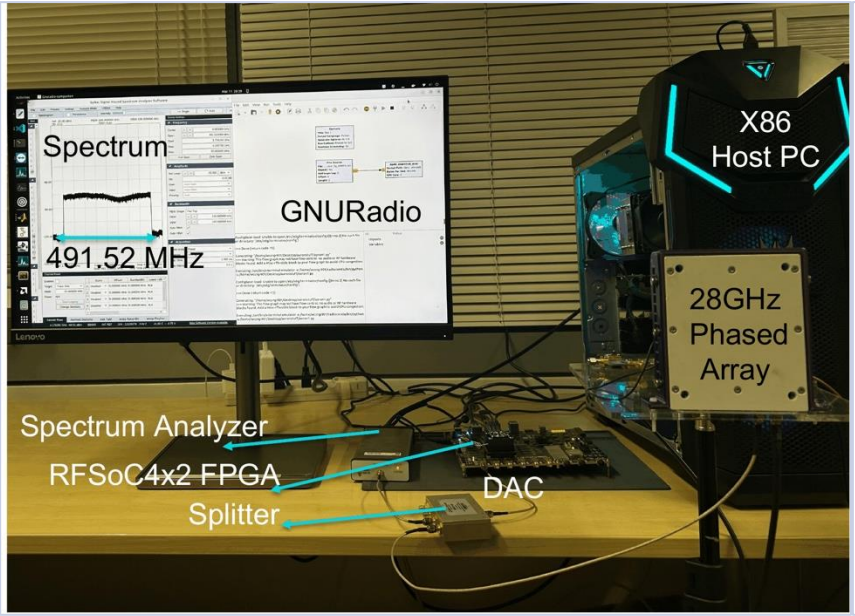
Uplink reliability against a commercial radio

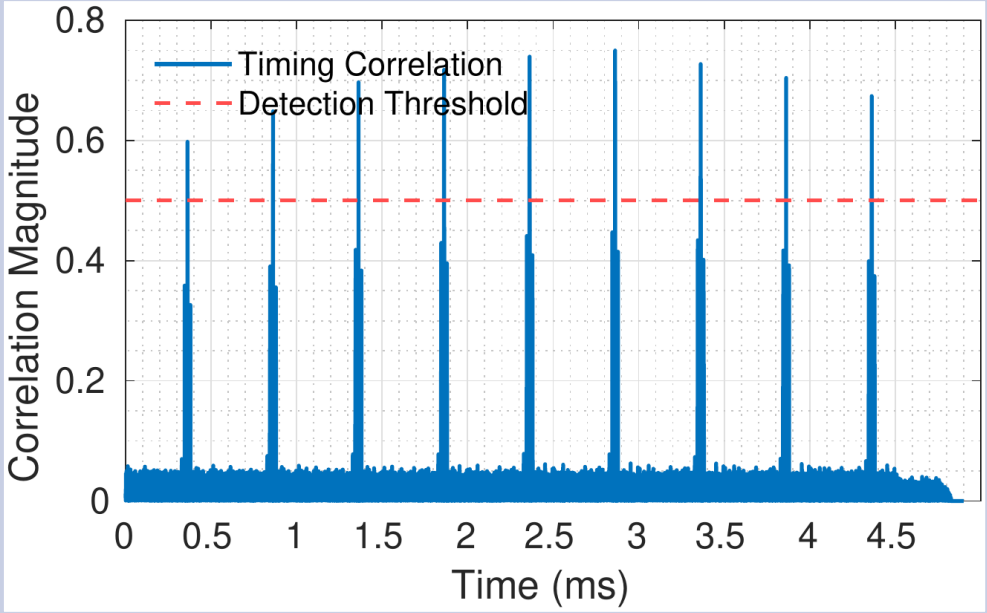
Aggregate uplink rate	USRP X410 + UHD 4.8	RadioStream
491.52 Msps	lossless	lossless
983.04 Msps (2 × 491.52)	0.0047% lost	0 samples lost
1966.08 Msps (4 × 491.52)	Fails with single 100G QSFP link	rate sustained, on 3 cores with single 100G QSFP link

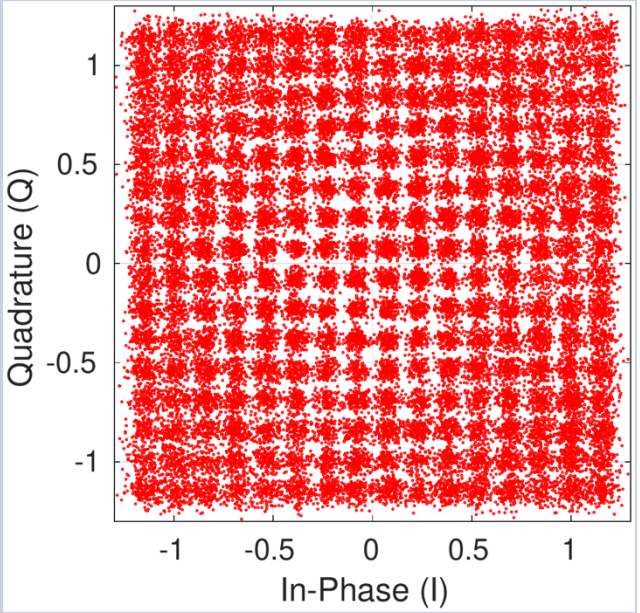
Where do the samples go?

- **The X410 Limit:** Even with 8 dedicated cores, UHD's host-timed transport lost samples. It could be due to buffering or insufficient number of cores.
- **The RadioStream Advantage 1 (Buffering):** PL-DDR4 provides a larger jitter budget. When the exact same OS stall happens, the deep memory absorbs it. The host catches up, and zero samples are lost.
- **The RadioStream Advantage 2 (Efficiency):** NO flow-control, the transport is just a simple memory pipe. The system easily sustains the rate on just 3 cores.

Application 1: Wideband Communication







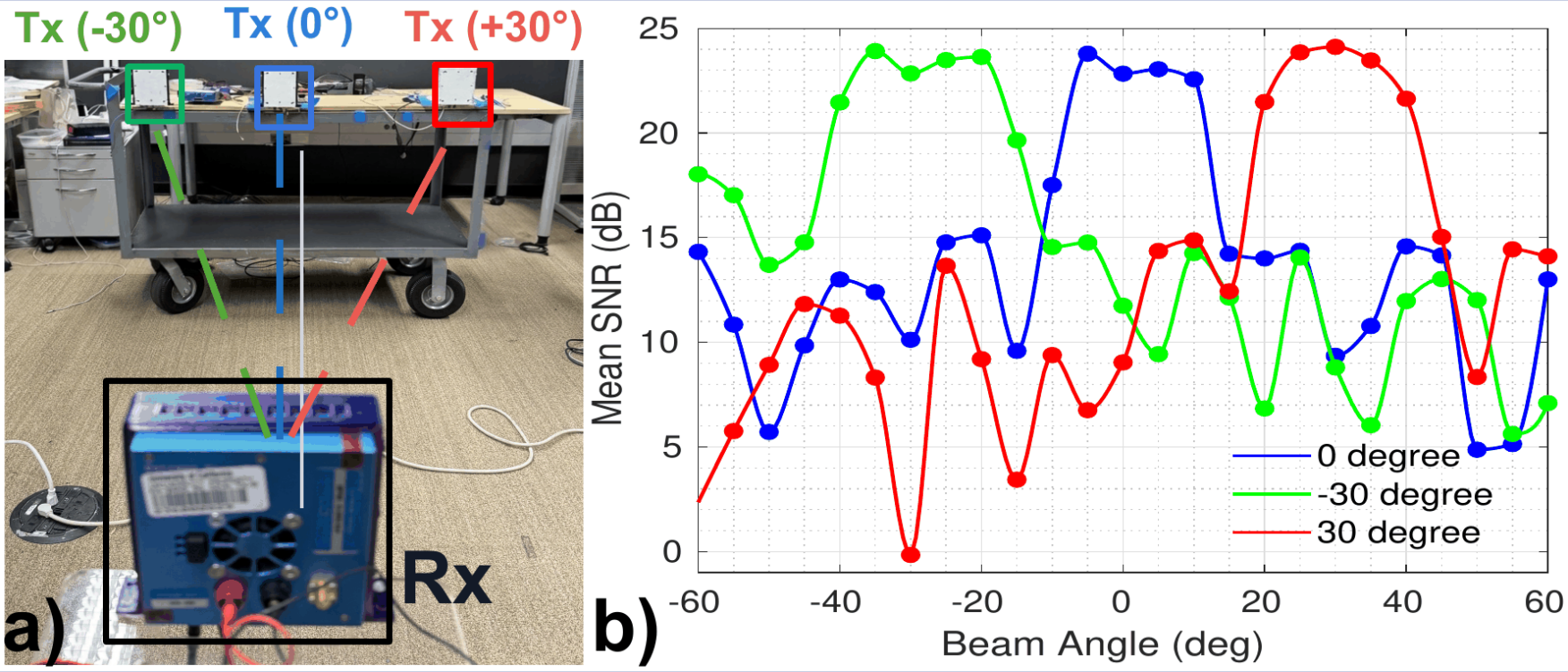
OFDM · 256-QAM
491.52 MHz IBW @ fc = 28 GHz

EVM 4-6%
flat across slot and resource block

491.52 MHz
WiFi-style OFDM at 4 GHz

Slot boundaries land exactly where they should, and the IQ between them is unbroken.

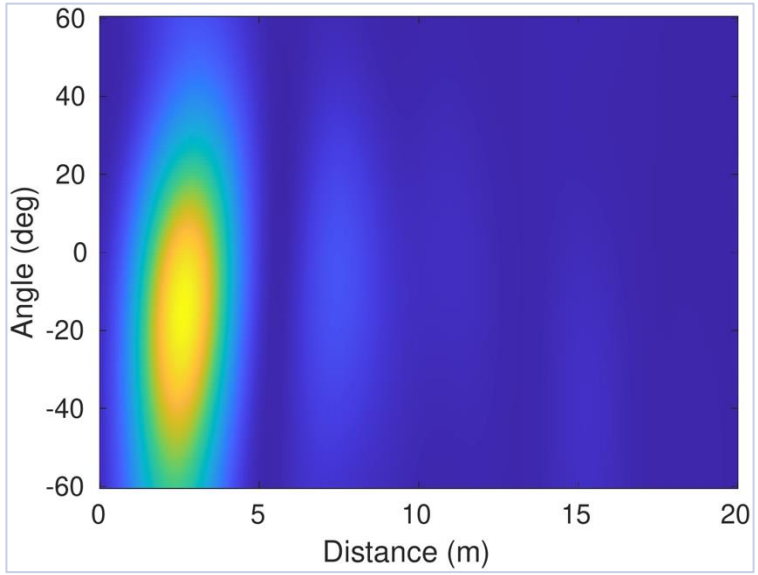
Application 2: 28 GHz mmWave beam sweeping



- RFSoC sweeps the beam while streaming continuously at 491.52 MHz.
- Peaks land on the three known transmitter angles.
- Steering happens per slot, on the wire already carrying the samples.

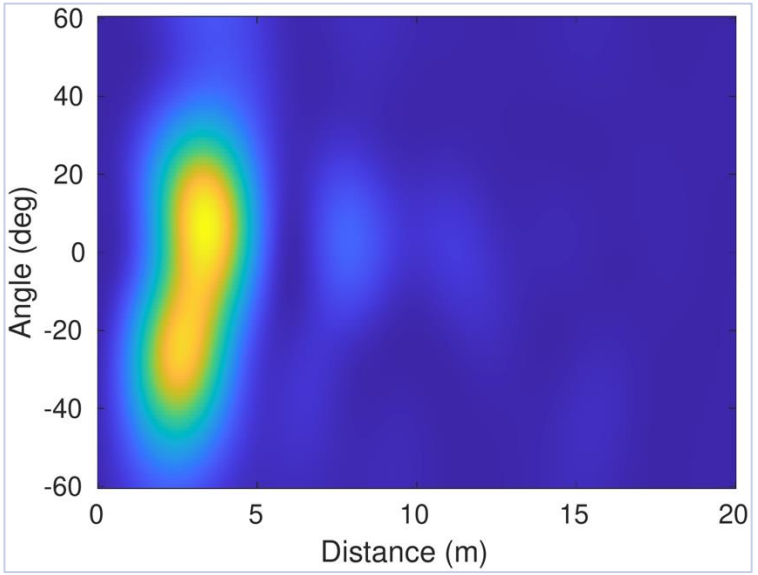
Application 3: sub-6 GHz AoA and range estimation

Two sources at 4 GHz; receive elements 3 cm apart.



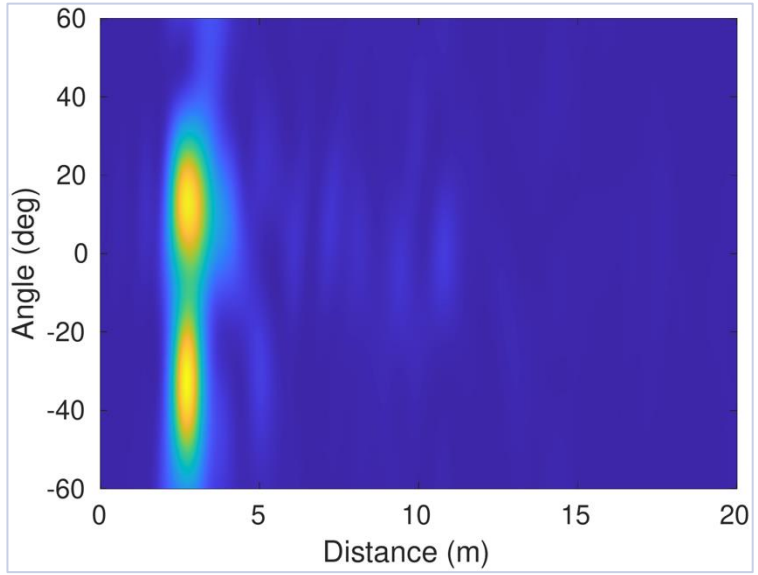
122.88 MHz · 2 antennas

the two sources merge



122.88 MHz · 4 antennas

angle resolves: 40° → 20°



491.52 MHz · 4 antennas

range resolves: 2.4 m → 0.6 m

Bandwidth buys range, antennas buy angle.

Wide bandwidth, many antennas and phase coherence all arrive over the same streaming path.

Takeaways

Exported radio time

The FPGA is the sole timing authority and ships each boundary to the host as a packet.

p99 jitter 598 ns

Explicit slot transport

Slot-tick, control and IQ are three separate, slot-addressable classes on one link;

90 Gbps, 0 drops

DDR based buffering

IQ samples are transferred two slots early and buffered in the FPGA to mask OS jitter

Two slot look-ahead notion

Limitations and what's next

- **Scaling past one link.** 8 ch × 491.52 MHz full-duplex is ≈126 Gbps; the second QSFP is already routed.
- **Full-stack integration.** srsRAN / OAI via a thin adapter - no FPGA or DPDK fast-path changes.
- **Multi-node sync.** The contract extends over a shared GPS/PTP reference; still open.

Thank you!

Questions?

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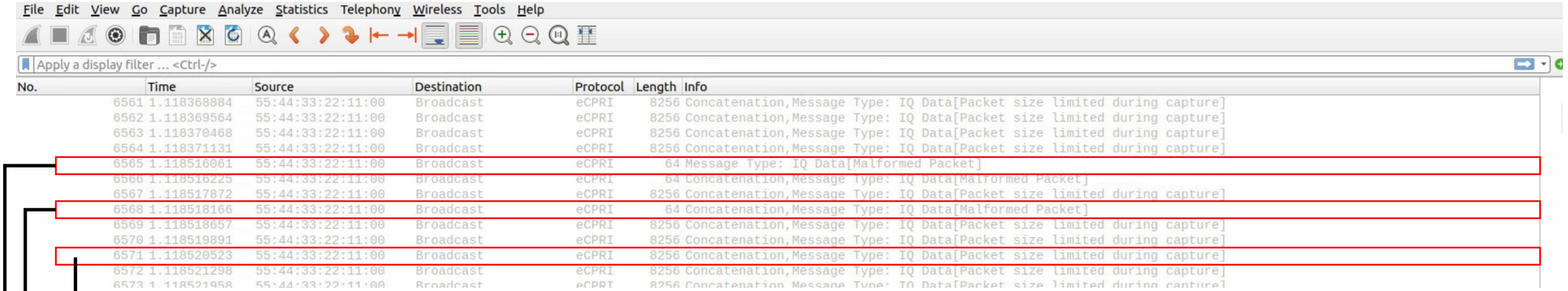
wcsng.ucsd.edu/radiostream

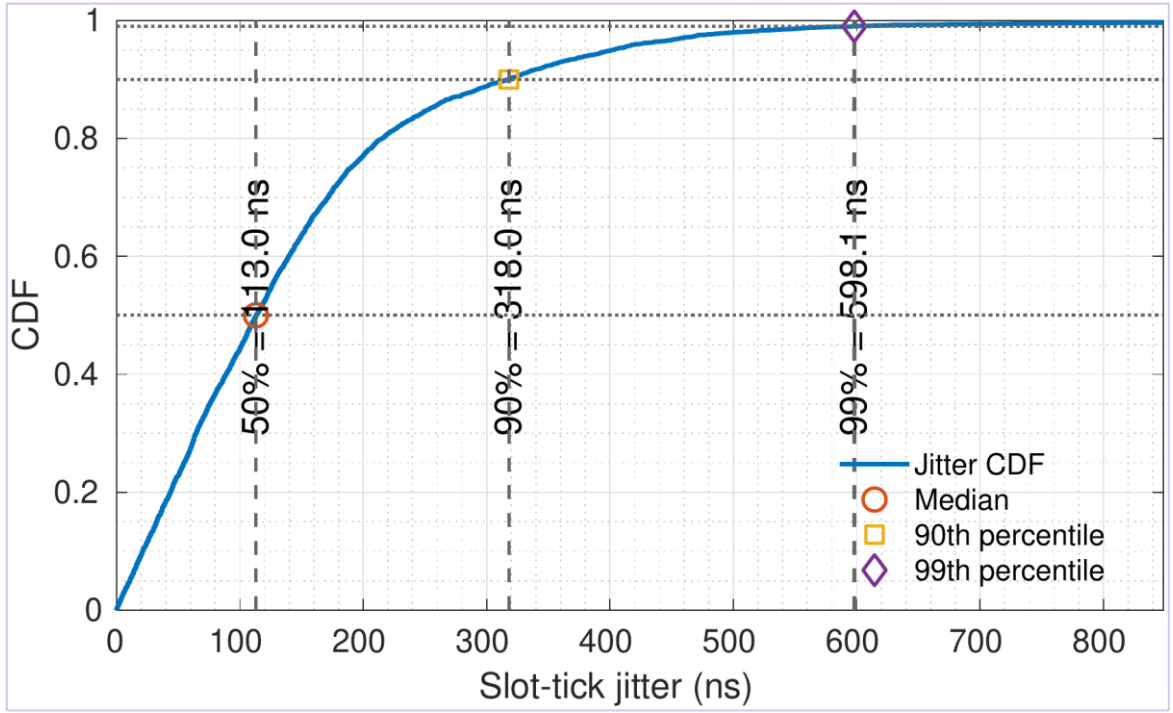
Three kinds of raw Ethernet packets on one link



Packet type	Direction	Size	Carries
Slot tick	FPGA -> Host	64 B	Current slot number. Exports radio time.
Data	Host -> FPGA (D) FPGA -> Host (U)	9000 B MTU	Uplink / downlink IQ, tagged (slot, direction).
Control	Host -> FPGA	64 B	Antennas, direction, NCO frequency, NCO phase.

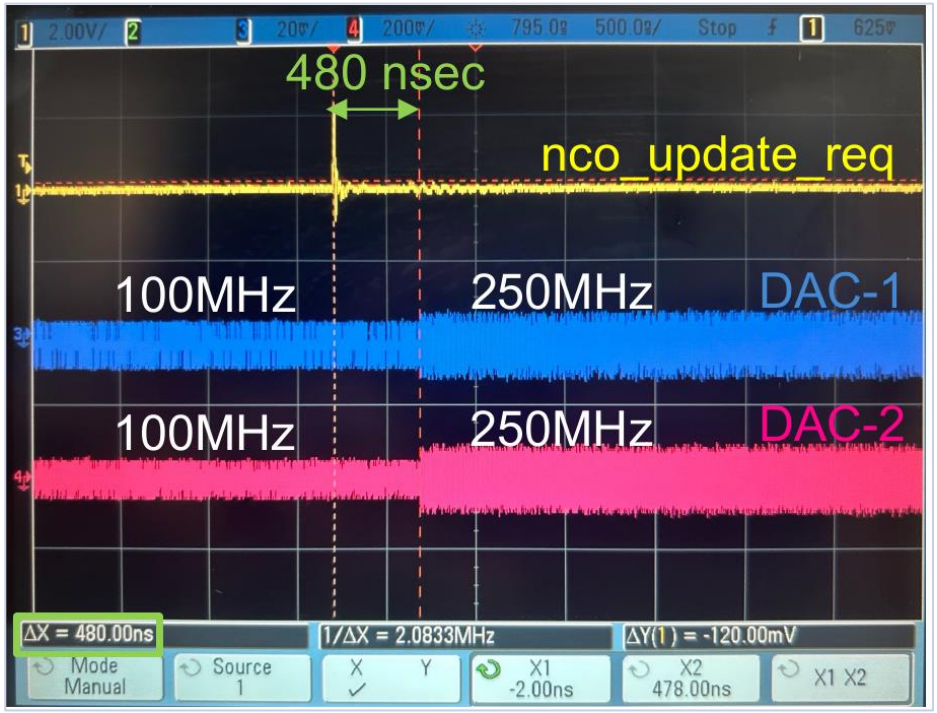
Timing accuracy and control latency

How accurately does the host see radio time?



median 113 ns | p90 318 ns | p99 598 ns

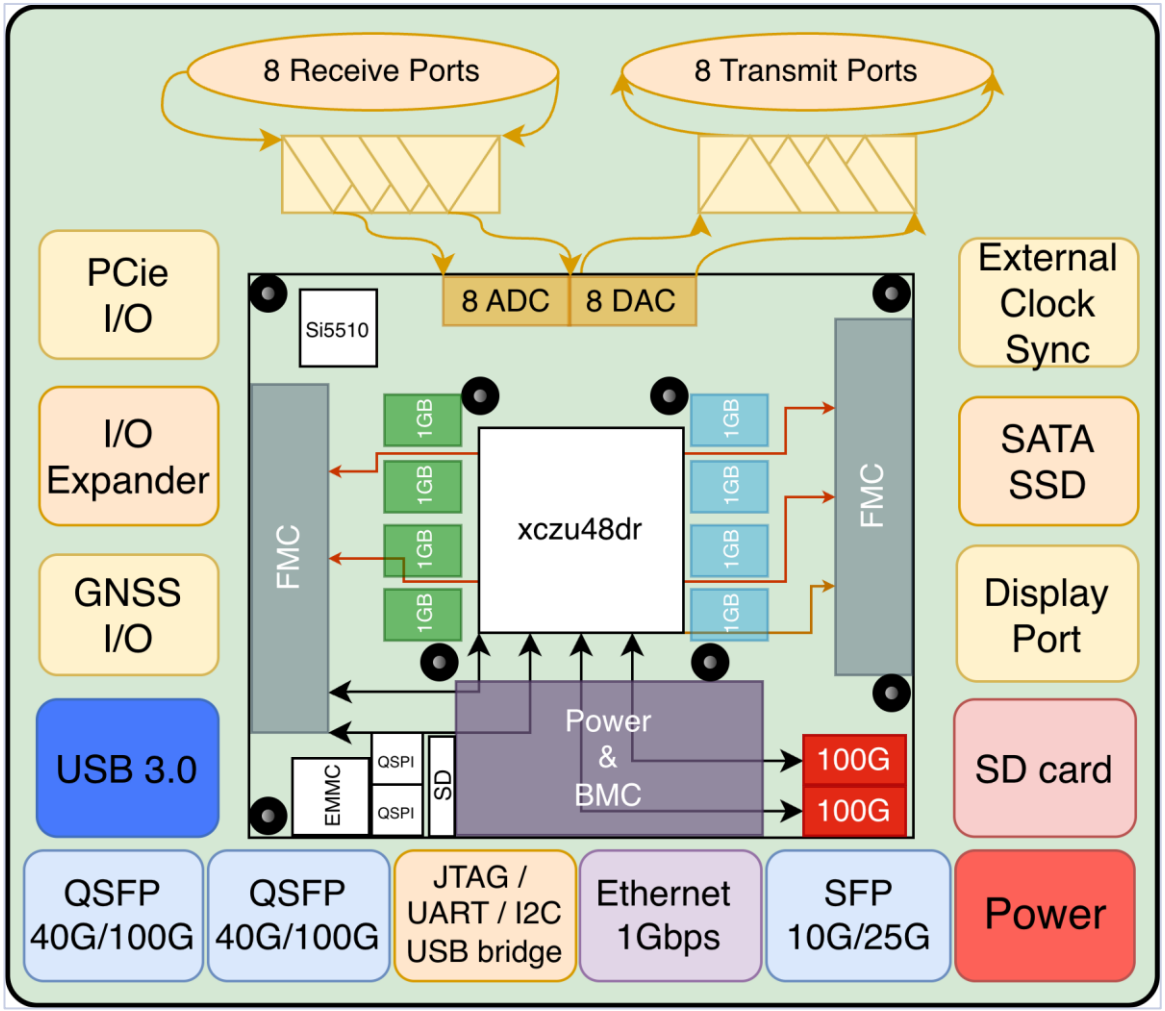
How fast does RF control command reach the air?



480 ns end-to-end - of which the RFDC update is 360 ns

Sub-µs on both sides: the host follows radio time to ~0.6 µs, and control lands at the RF output in under 0.5 µs.

The SOM and RF carrier board



System-on-Module

- **xczu48dr** - 8 ADC to 5 GSps and 8 DAC to 9.85 GSps, each through its own gain stage.
- **4 GB of DDR4 on the FPGA side** - this is where the slot buffers live.
- **Two 100 Gb ports** - we use one. The second is the headroom for 8 channels at full width.

RF carrier board

- Breaks out all 16 RF chains, both QSFP28 cages, PCIe x8, GPS in and management Ethernet.

8T8R
transmit / receive

2 × 100G
Ethernet ports

4 GB
PL-side DDR4

One clock circuit feeds GPS or PTP to every converter tile - that is what makes the channels phase-coherent.