New Capabilities for Comms, Radar, & EW with an SDR-based Research Platform

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Evolution of the Wireless World

Transforming All Industries

Software-Defined Solutions

High-Performance Requirements

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Higher Frequency

Wideband

Multi-Channel

Evolving Application Requirements of 5G and Beyond



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Enabling Technologies That Could Drive 6G

Evolution of MIMO

Build on multi-antenna techniques from 5G with more elements and distributed architecture.

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Sub-Terahertz

Utilize extremely wide bandwidths at frequencies once thought impractical for commercial wireless.

4G

Joint Communications and Sensing

Improve spectral usage by combining sensing and radar functions with communications channels.

Machine Learning and Artificial Intelligence

Leverage new techniques across all 6G - from the signal chain to the network topology.







USRP Product Portfolio Overview

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Ettus Research Attinue Rese	Ettus Research USRP B2XX	Ettus Research USRP N310 / N32X	Ettus Research USRP X310	Ettus Research USRP E320	NI Ettus USRP X410
Frequency	70 MHz – 6 GHz	3 MHz-6 GHz (N32X) 10 MHz-6 GHz (N310)	*10MHz – 6 GHz	70 MHz – 6 GHz	1 MHz – 8 GHz
Bandwidth	56 MHz	200 MHz (N32X) 100 MHz (N310)	*160 MHz	56 MHz	400 MHz
Channels	2 Tx, 2 Rx	2 Tx, 2 Rx (N32X) 4 Tx, 4 Rx (N310)	2 Tx, 2 Rx *4 Rx (TwinRx)	2 Tx, 2 Rx	4 Rx, 4 Tx
RF Performance	Good	Best	Best	Good	Better
Architecture	Integrated	Integrated	*Configurable w/ Daughterboards	Integrated	Integrated
Communication	USB	10 GbE or PCIe	10 GbE or PCIe	10 GbE	100/10/1 GbE or PCIe
Synchronization	2x2 MIMO	Up to 128x128 (N32X) Full Phase Synchronization	*2x2 MIMO	2x2 MIMO	4x4 MIMO
SW Support	GNU Radio, C++, Python, MatLab, LabVIEW	GNU Radio, C++, Python, MatLab, RFNoC	GNU Radio, C++, Python, MatLab, RFNoC, LabVIEW, LabVIEW FPGA	GNU Radio, C++, Python, MatLab, RFNoC	GNU Radio, C++, Python, RFNoC, LabVIEW *Q4 2021
Key Features	Low SWAP-C, Highly portable	Stand Alone, Wide bandwidth, Multi-Channel Sync Ready (N32X)	*Configurable RF Front End, Programable FPGA	Low SWAP, Embedded Deployable, Standalone	RFSOC Based, 5G Ready, Wide Band, Multi-Channel

NI Ettus USRP X410 Product Overview

RF Capabilities

Frequency Range:	1 MHz - 8 GHz		
Signal Bandwidth:	400 MHz		
Receive Channels:	4X		
Transmit Channels:	4X		
Max TX Power:	up to 22 dBm ¹		
Max RX Power:	0 dBm		

¹ see specification for details

Digital Capabilities

PHILIP

Xilinx Zynq Ultrascale+ RFSOC Built-in quad core ARM processor Onboard IP: SD-FEC, DDC, DUC Interface options: dual QSFP28, PCIe Gen 3 x8² Synchronization: 10 MHz / PPS, GPS DO option Software:

Open source (GNU Radio, RFNoC, UHD) NI-USRP², LabVIEW FPGA²

² available in September 2021





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The NI Ettus USRP X410 | Hardware Features



The NI Ettus USRP X410 | Software Features



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USRP/FlexRIO FPGA Resource Comparison





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USRP X410 Overview – Front Panel



USRP X410 Overview – Rear Panel



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Radar/EW Research Platform for SDR



Radar/EW Research Platform for SDR

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Radar/EW Research Platform Reference Architecture

- Enables radar/EW researchers struggling to rapidly prototype new concepts to move quickly from software simulation to hardware demonstration, ultimately turning novel concepts into fielded capability faster
- Key Features
 - Direct Conversion RF Sampling (200 MHz IBW) with NI USRP (L, S, C band)
 - Coherent operation through duration of experiments w/ LO, RefClk, and PPS sharing
 - 32 Channel TxTx,RxRx,TxRx Synchronization and Streaming (Ref C++ code, System Configuration)
 - Waveform Generation from File (C++) using RFNoC Replay blocks
- Multiple open-source software programming options, including C++ and Python
- System specification datasheet for array synchronization and waveform generation/acquisition example code for USRP
 - Repeatability better than 10deg, Stability better than 1deg
 - Target: Full rate streaming 8 channels, reduced rate streaming at higher channel count
- Documentation for integrating GPU-based DSP and MATLAB Host programming
- NI-Supported Code available for open-source access on GitHub
- NI Technical Consulting Services for project acceleration and risk mitigation





Getting from the Whiteboard to Proven Concept



Develop and simulate algorithms and system in software Develop hardware test bed, iterate with offline processing, migrate processing to hardware Validate algorithms against simulator and real-world scenarios, iterating as necessary Migrate validated algorithms to mission hardware, perform integration testing/validation

USRP N320 / N321

Common:

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3 MHz - 6 GHz range 200-MHz BW per channel 2X2 MIMO 200/245.76/250-MHz sample rates Preselection filters Dual SFP+ ports (1 GbE, 10 GbE, Aurora) QSFP+, RJ45 GPSDO Ethernet-based sync (White Rabbit) Stand-alone operation



N320:

Zynq XC7Z100-2FFG900I External LO input ports

N321:

LO Distribution for up to 128x128 MIMO





LO Distribution CCA Inside The N321

Star LO Distribution

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Support up to 128x128 MIMO



CLOCK DISTRIBUTION SOURCE

Software Architecture of Reference Architecture



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Hardware Architecture of Reference Architecture



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Data Movement and Synchronization





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