
Adventures in RFNoC™: Lessons Learned From Developing a Real-Time Spectrum Sensing Block

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Abstract

The RF Network-on-Chip (RFNoC™) is an open source framework from Ettus that allows for convenient development access to the field-programmable gate array (FPGA). The RFNoC framework therefore lowers the barrier to entry to develop FPGA based digital signal processing (DSP) blocks that can be used with UHD and GNURadio (Ettus, 2018). By utilizing the floor space available on the FPGA of select radio models, DSP can be done in hardware before the data is ever streamed to the host computer. This type of heterogeneous processing can increase the speed of computationally intensive algorithms by helping to parallelize operations on the FPGA prior to generalized processing on the host computer. In addition to computational savings, deploying algorithms to the FPGA can reduce latency by removing the need to send data to the host computer or by reducing the amount of data that needs to be streamed to and processed by the host computer.

This presentation and the accompanying paper discuss the lessons learned from RFNoC development on the Ettus X310 radio. We will describe the framework and implementation architectures that reduced development time and enabled complex algorithms to be run in real-time. The AXI-Stream Payload Context interface was selected for the development of the processing blocks. A brief overview of this interface is discussed along with methods for sending block-generated packets.

The blocks that are presented in this work are for the implementation of fast spectrum sensing (FSS) (Kirk et al., 2018) for dynamic spec-

trum sharing applications. FSS operates by taking a sample of the spectrum and then looks for the largest band that is unoccupied by the primary users and can be utilized by the radio's application. Due to the time-frequency agility of modern communications networks, the radio must be able to sense a new primary user in sub millisecond timescales in order to minimize interference. We will demonstrate two different detection methods for checking for a signal in each frequency bin of an FFT frame. As previously mentioned, FSS is a speed critical application, as a new emitter could begin transmitting at any time and the system would need to jump out of the way and select a new sub-band. Because of this the FSS algorithm needs to be implemented in the FPGA to minimize processing time and reduce streaming data and latency requirements to and from the computer. Minimizing the processing and data requirements ensures that the system can run the algorithm on each frame of data as quickly as possible such that a transmit waveform selection algorithm always has the most recent spectrum estimate.

A block architecture is presented for two versions of the FSS algorithm. The first allows for the implementation of a simpler algorithm with a predetermined threshold, that only needs to see each sample once and allows data to continue through the passthrough port of the block uninterrupted. The second architecture discussed enables a more robust algorithm that needs to calculate the threshold before it is applied. This is accomplished through caching of packets to allow for the data to be accessed or iterated over multiple times by the algorithm. Much of the input and output timing complexity usually associated with developing streaming FPGA IP is shouldered by RFNoC which allows for a more singular focus on the algorithm implementation. Is-

sues that were encountered with these implementations within this framework will be described and the throughput and bandwidth performance will be discussed and demonstrated.

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References

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